

SECTION 7

DETECTOR UN20/507

Introduction

The UN20/507 as used in a Television Automatic Monitor Minor MN2M/508 (see Instruction V.11) accepts as inputs a clamped video signal and gated portions of selected sync pulses. Relays are released if either the amplitude of the video signal or the noise level in the gated sync pulses lies outside certain limits. The UN20/507 also contains an 800-kHz oscillator which is used in the Automatic Monitor for self-checking.

The UN20/507 is constructed on a CH1/12A chassis with index peg positions 1 and 35.

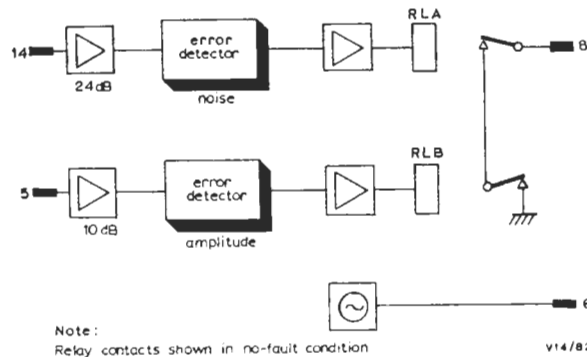


Fig. 7.1 Block Diagram of the UN20/507

General Description

Fig. 7.1 shows a block diagram of the UN20/507 which comprises an 800-kHz oscillator and two voltage error detector circuits. These detectors have a characteristic of the type shown in Fig. 7.2. The output relay releases if the input amplitude departs from its correct value.

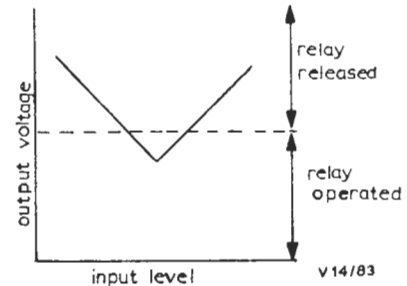


Fig. 7.2 Characteristic of Error Detector Circuits

Circuit Description

The circuit of the UN20/507 is shown in Fig. 7.3. The noise error detector circuit which includes transistors TR1 to TR12 and TR23 has an input amplifier in two parts separated by a weighting network (resistor R14 and capacitor C8). The first part of this amplifier is a simple negative-feedback amplifier. The second part, sometimes known as a super emitter follower, is similar to many power supply regulating circuits (see Fig. 7.4).

The input amplifier is followed by a voltage-doubling peak-rectifier and a long-tailed pair. An output is taken from the more positive collector of the pair, giving the characteristic shown in Fig. 7.2. This output is fed to a two-stage relay-drive amplifier.

The video-amplitude error detector circuit is similar to the noise error detector after the weighting network.

Test Procedure

The UN20/507 is tested as part of an MN2M/508 or MN2M/508A.

See page 7.3. for Fig. 7.3.

See overleaf for Fig. 7.4.

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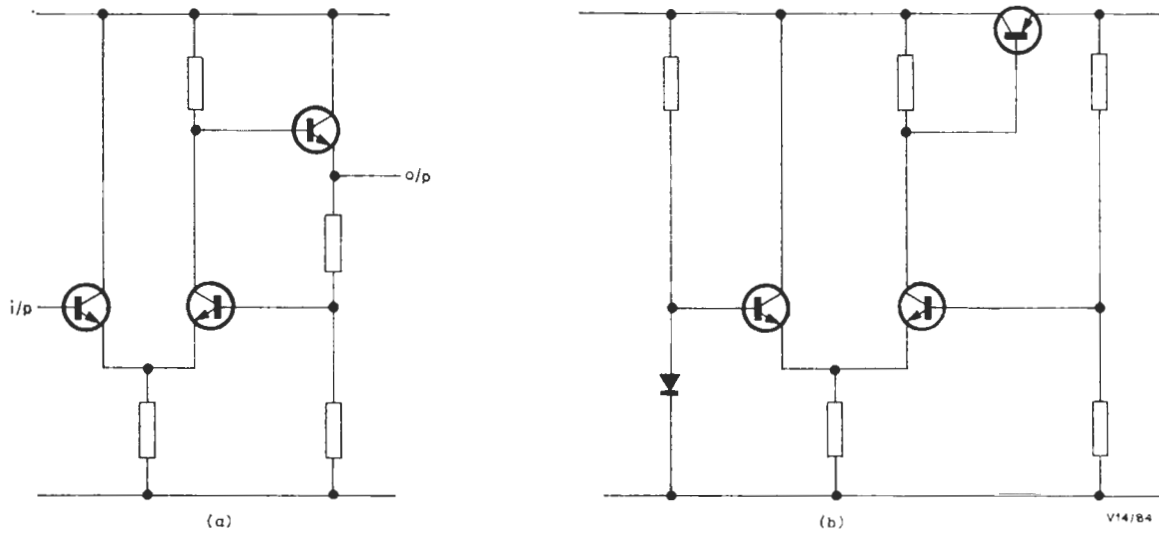
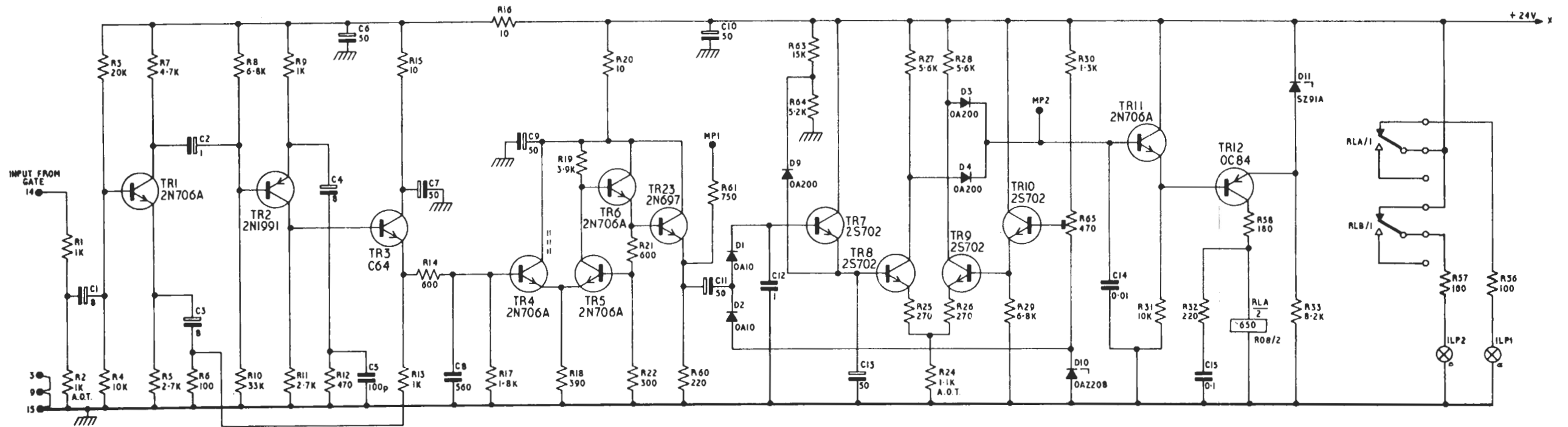
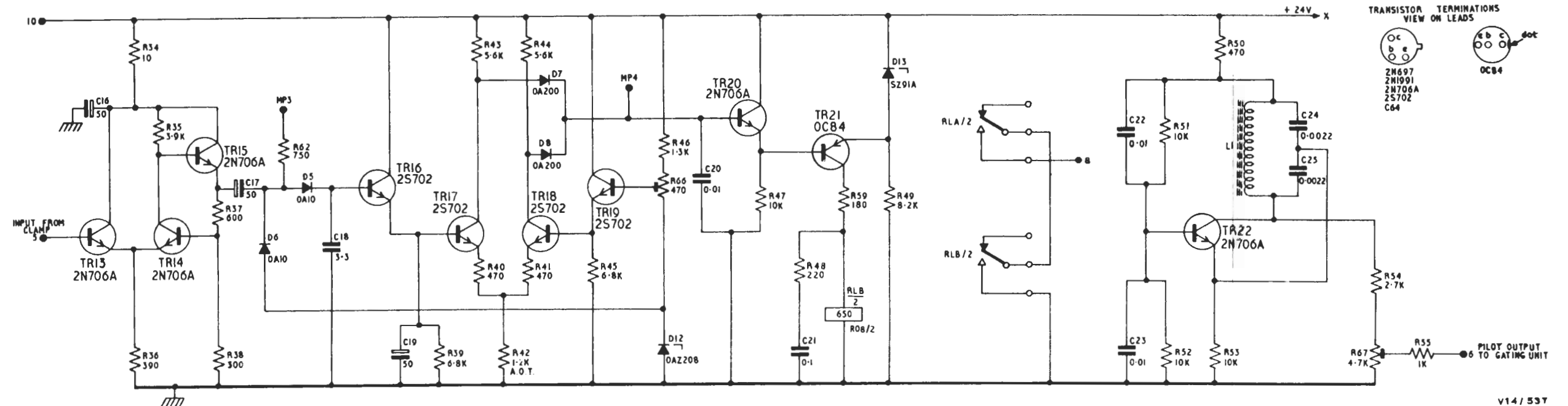


Fig. 7.4 Comparison between (a) Super-emitter-follower and (b) Stabilised Power-supply Circuits

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Fig. 7.3 Circuit of the UN20/507