CHROMINANCE AND SYNC PULSE AMPLITUDE DETECTOR UN20/518

Introduction

The UN20/518 accepts inputs of one sync pulse per field and the chrominance bar component of an Insertion Test Signal waveform and provides d.c. outputs corresponding to the amplitude of each input.

The unit is built on a printed wiring board and mounted on a CH1/43 chassis.

Principle of Operation (Fig. 1)

Fig. 1 shows the basic form of amplitude detector.

A pulse is applied to one input of a differential amplifier and a voltage fed back from the output of the detector is applied to the other input. If the input pulse is greater in amplitude than the fed-back signal, the differential amplifier produces an output which triggers a monostable multivibrator. An output pulse from the monostable is applied to a diode pump and buffer amplifier. When the amplitude of the fed-back voltage equals the amplitude of the direct input, the output of the differential amplifier falls to zero. The output from the detector is a direct voltage the level of which is proportional to the amplitude of the input pulse.

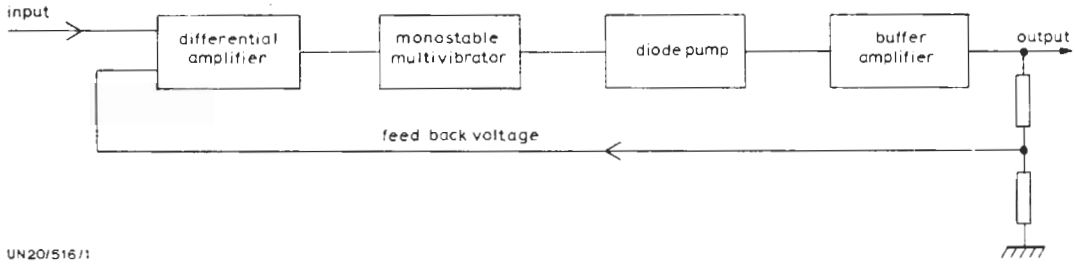

Fig. 1. Basic Circuit of the Amplitude Detector

General Specification

Inputs

One sync pulse per field	0·9 volt p-p across 225 ohms.
I.T.S. chrominance bar	1·4 volts p-p across 75 ohms.

Outputs 5 volts d.c. if the input is at the specified level.

Logic Levels

Logic 0: input	0·8 volt max.
output	0·4 volt max.
Logic 1: input	2 volts min.
output	2·4 volts min.

Power Requirements +6 volts at 8 mA
+12 volts at 4 mA
−12 volts at 5 mA

Continued overleaf

Circuit Description (Fig. 2)

Fig. 2 is a circuit diagram of the UN20/518. The sync pulse and the chrominance bar measuring sections of the circuit are separate but they function in an identical manner.

Sync Pulse Measuring Detector

The sync pulse to be measured is applied through pin PLA5 to the base of transistor TR4. The output from the collector of TR4 is applied to the non-inverting input of an integrated differential amplifier IC3. The inverting input of the amplifier is fed with a voltage derived from the d.c. output of the detector.

If the sync pulse input to IC3 exceeds the fed-back voltage, the amplifier produces an output which is applied to a common-emitter amplifier TR5. Part of the output from TR5 is fed to the inverting input of IC3 via C13 and R27. The effect of this is to cause IC3 to act as a monostable circuit, the sync pulse input being in effect a trigger signal. The output from the differential amplifier is a pulse of constant width and amplitude which depends upon the difference between the two inputs. This pulse is fed through TR5 to a diode pump circuit comprising capacitors C14 and C15 and diodes D5 and D6.

A direct voltage is built up across capacitor C15 and is applied to the base of transistor TR6 which together with TR7 forms a complementary emitter-follower.

The fed-back voltage to the differential amplifier is set by variable resistor R33. A small positive offset voltage is applied to the feedback circuit via resistor R35 to ensure that the monostable action is reliable.

I.T.S. Chrominance Bar Measuring Detector

The action of this part of the circuit is almost identical with that previously described. The only difference is that a conventional monostable arrangement is used. The output from the differential detector IC1 is applied to two cross-connected NAND-gates IC2a/2 and IC2b/2 which form the monostable multivibrator.

Setting-up Procedure

The unit is tested as part of its parent equipment.

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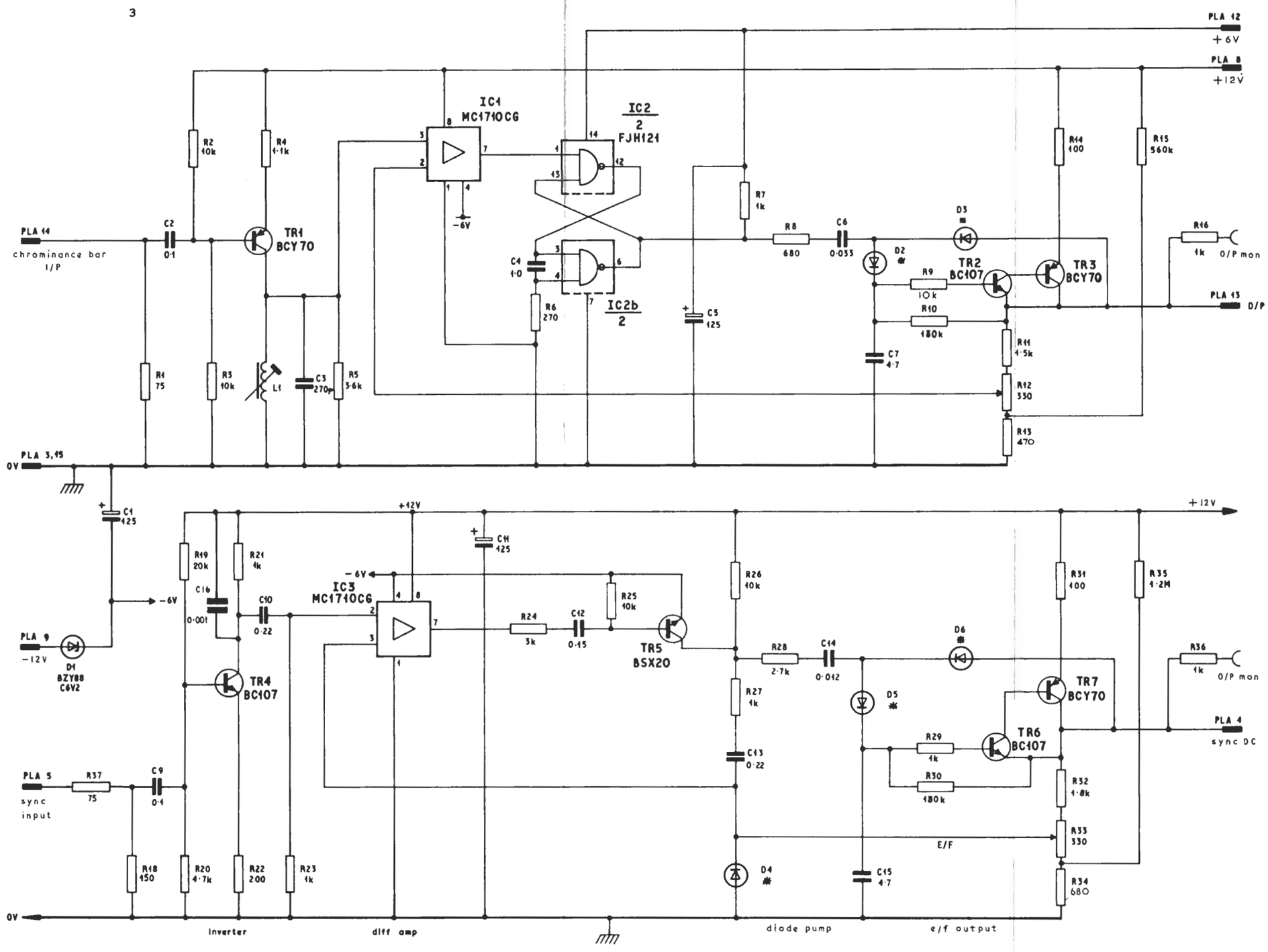
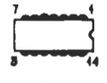


transistor terminations
view on leads

BC107
BCY70
BSX20
} collector connected to envelope

integrated circuit terminations
view on top



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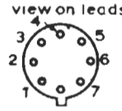
view on leads



MC1710CG

* D2-D6 IN4148

UN20/518/1T

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parts list D24446A4

Fig.2. Circuit of UN20/518