NOISE AND FLASHING DETECTOR UN20/519

Introduction (Fig. 1)

The UN20/519 accepts the following inputs:

(a) 1-volt p-p video signal.

(b) Positive-going 2-μs clamp pulses timed to occur during the back porch period.

(c) A 10-μs negative-going trigger signal; the leading edge of the trigger signal must be coincident with the leading edge of the line-sync pulse on lines 12 and 325.

(d) D.C. signals corresponding to the amplitude of an I.T.S. luminance bar and sync-pulse amplitude; 5 volts if the bar and pulse amplitudes are correct.

The output from the unit is a direct voltage the value of which is related to the level of noise and flashing on the video input signal. Fig. 1 is a calibration curve for the unit.

The unit is built on a printed wiring board which is mounted on a CH1/43 chassis.

Brief Specification

Inputs	(a) Composite video signal, 1 volt p-p (b) 2-μs clamp pulses, 12-volts p-p. (c) Line-trigger pulses, 5-volts p-p, on lines 12 and 325.
Outputs	
Noise	Direct voltage varying between zero and 7·5 volts positive. (5 volts are equivalent to unweighted noise level of 31 dB.)
Flashing	Output rises to 8 volts positive in presence of flashing.
Power Requirements	+12V at 60 mA −12V at 60 mA +6V at 10 mA

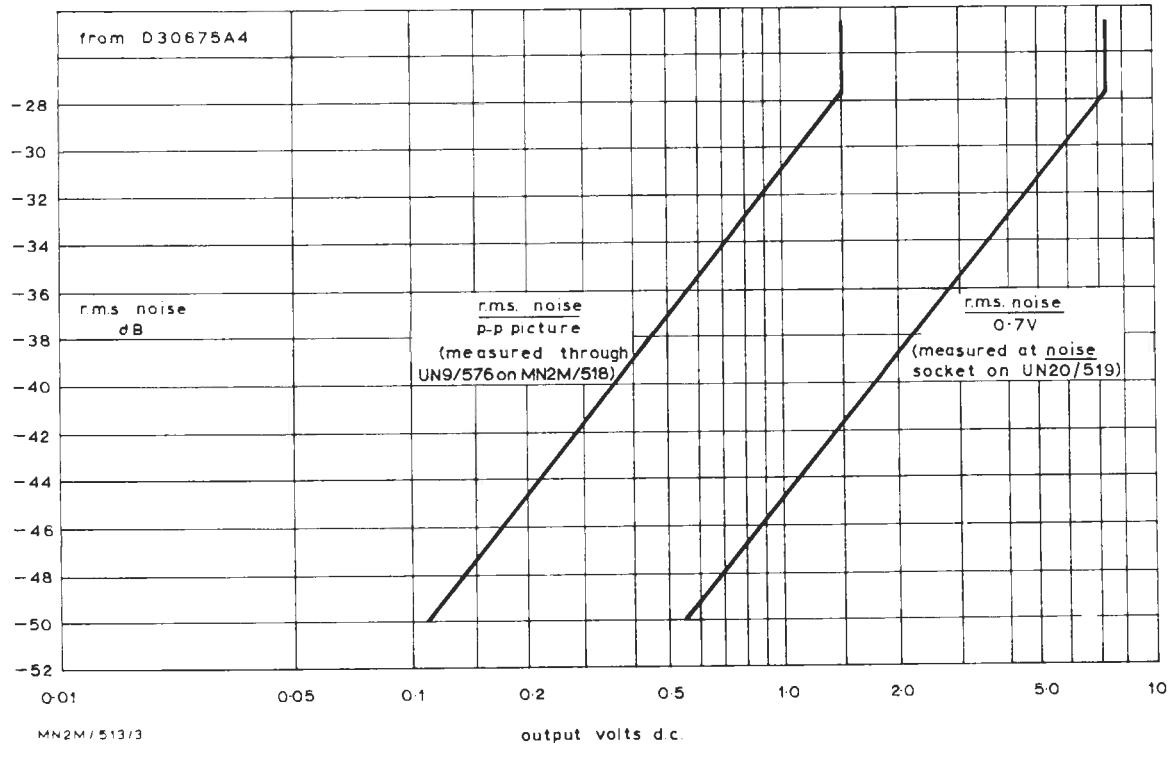

Fig. 1. Calibration Curve

Circuit Description (Fig. 2)

Fig. 2 is a circuit diagram of the UN20/519.

For the purposes of the following description the circuit is considered as a number of separate sections.

Video Input

The video input is applied through pin PLA6 to the base of transistor TR1. Transistors TR1 and TR2 together form a high-input-impedance stage. The signal from the collector of TR2 is fed through capacitor C2 to the base of transistor TR4 where, during the back porch period, it is clamped to earth potential.

The clamped signal is fed to transistors TR4 and TR5 and to the source of f.e.t. TR6. Transistors TR4 and TR5 are both emitter-follower amplifiers. The signal from TR5 is taken through matching and low-pass filter components to the flashing-detector circuits.

2-μs Clamp Pulse Amplifier and Switch

Positive going two-microsecond clamp pulses, timed to occur during the back porch period, are applied through PLA10 to the base of emitter-follower TR16. The pulses from TR16 operate switch TR3 whose collector is connected to the base of transistor TR4.

40-μs Gating Pulse Generator

A trigger signal corresponding to the start of line 12 and 325 is applied through pin PLA4 to TR17 a common-emitter stage. The signal from TR4 triggers a monostable circuit IC2 which produces a negative-going pulse about 40 μs wide. The monostable output is applied to the base of transistor TR18, which forms a differential amplifier with TR19. The base of TR19 is held at a constant potential and the outputs are positive and negative going pulses which are applied to the gate of f.e.t.s TR6 and TR7 respectively.

Gating Circuit

During the 40-μs gating pulses, f.e.t. TR6 is saturated and f.e.t. TR7 is cut off, and the selected part of line 12 or 325 is passed to the base of TR8 which with TR9 forms a high-input-impedance circuit the same as TR1 and TR2. The output from TR9 is passed to one input of a differential amplifier IC1 through a 5·8-MHz low-pass filter. The filter restricts the bandwidth so that only in-band noise is measured.

Differential Amplifier IC1

The signal from TR9 is fed to the inverting input and the non-inverting input is fed with a voltage controlled by variable resistor R35 from the output of the unit. If the voltage at the inverting input exceeds the fed-back voltage, the differential amplifier produces an output. If the two input voltages are equal there is no output. The signal from IC1 is applied to a common-emitter amplifier TR10 and to a diode-transistor pump.

Diode-transistor Pump

The diode-transistor pump comprises C10, D4 and TR11. A direct voltage is built up across C10 depending upon the output from the differential amplifier. This voltage is transferred to the gate of f.e.t. TR12 during the periods D4 is not conducting. A 10-μs negative-going gating pulse, from the collector of transistor TR21, is applied to the gate of TR12. F.E.T. TR12 conducts only when the pulse is absent. TR12 and TR14 together make a high-input-impedance stage, and TR13 is a constant-current generator to feed the source of f.e.t. TR12.

Output Stage

The base of TR15, an emitter-follower, is fed with signals from the output of TR12 and also from the output of the flashing-detector section of the circuit. The output signal is connected to pin PLA9.

10-μs Gating-pulse Switch

The positive-going 10-μs line-trigger input from the collector of TR17 is taken to the base of TR20, a common-emitter amplifier, and then via TR21, a common-base amplifier, to the collector of TR11. Transistor TR11 can conduct only when the gating pulse is present.

Flashing Detector

A direct voltage corresponding to the level of a measured sync pulse is fed through pin PLA13 to the inverting input of a differential amplifier IC3. IC3 is connected as an inverting amplifier. The output from IC3 is taken to the non-inverting input of one amplifier of a dual differential amplifier IC4. The inverting input of the other section of IC4 is fed with a direct voltage, via pin PLA14, which corresponds to the amplitude of the I.T.S. luminance bar. The other input of each section of the dual amplifier is fed with clamped video signal from the emitter of TR5.

The output of each section of the dual amplifier is connected through R62, R63 and C20 to the base of common-emitter amplifier TR22.

Amplified negative feedback is applied to this stage through a common source amplifier TR23. The signal from TR22 is passed through common-emitter amplifier TR24 to the base of the output stage TR15. Transistor TR25 is a constant current generator for TR24.

Test Procedure

The UN20/519 is tested as part of its parent unit.

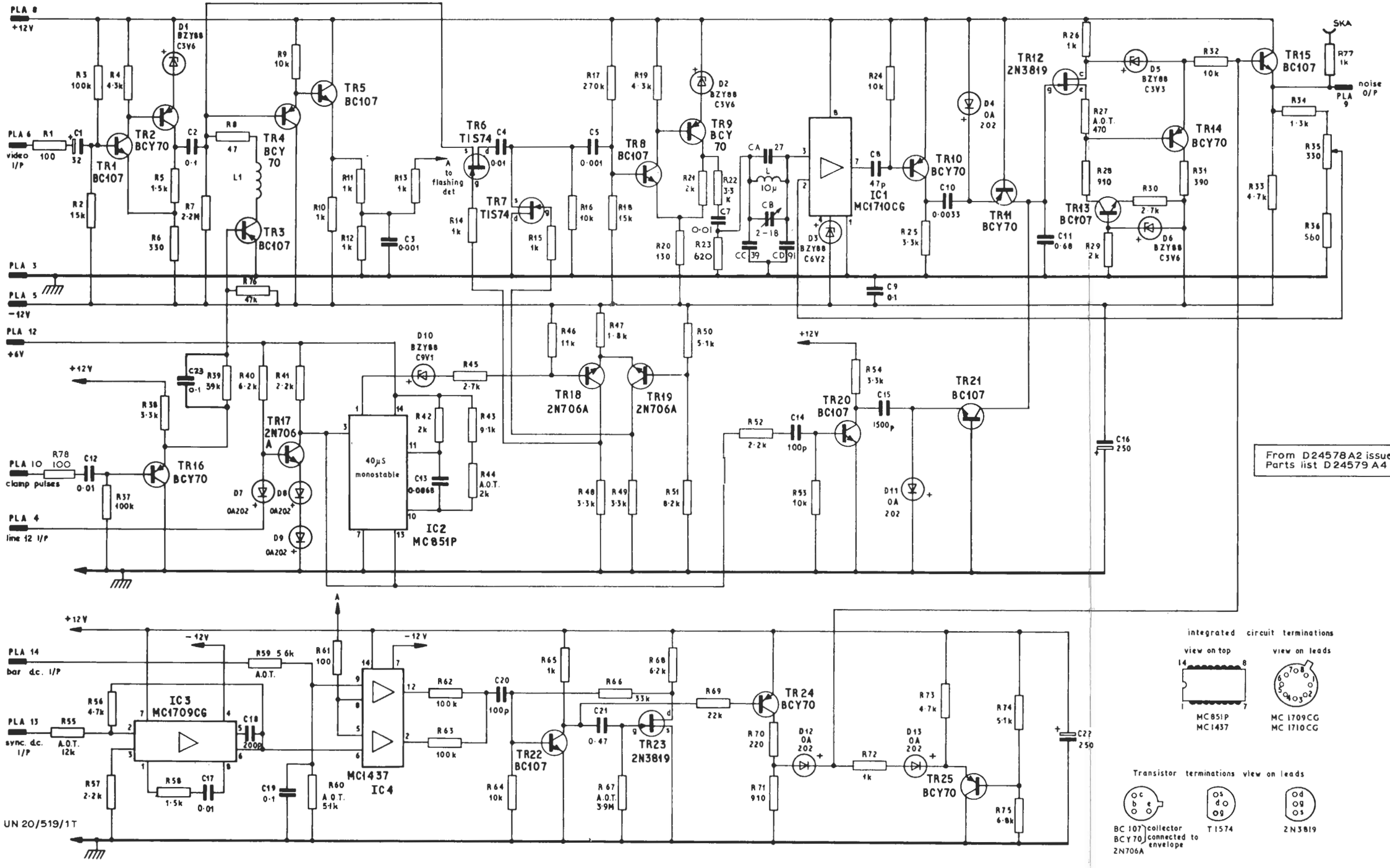

Fig.2. Circuit of UN20/519