# SOUND-IN-SYNCS ERROR DETECTION UNIT UN20/527

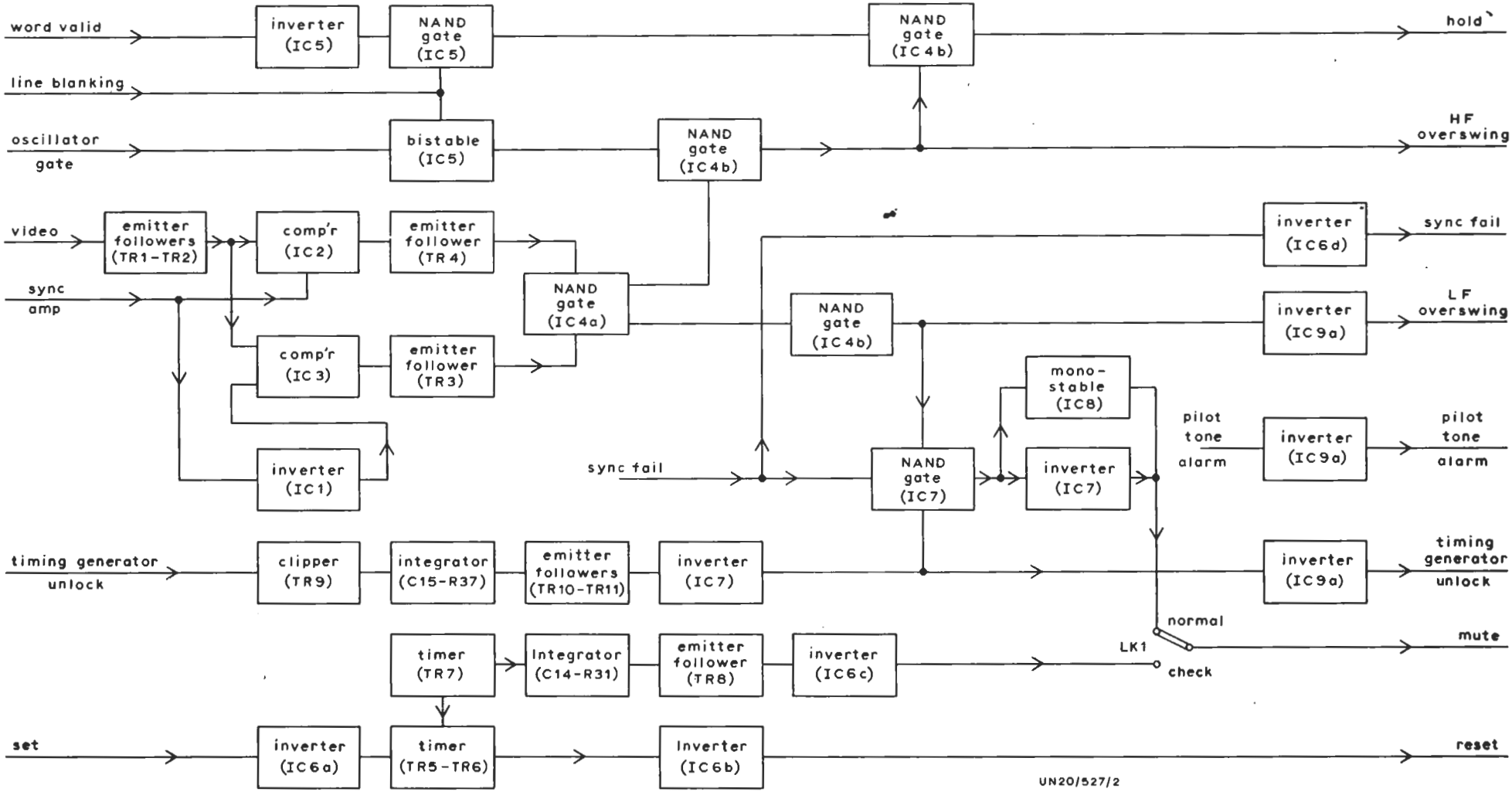



*Fig. 1 Simplified Block Diagram of the UN20/527*

## Introduction

The UN20/527 forms part of a sound-in-syncs decoder[1]. The unit processes various analogue and digital signals generated within the decoder in order to detect fault conditions. The outputs of the fault detection circuits are combined and applied to Mute and Hold circuits which, when fault conditions exist, feed inhibit signals to the digital-to-analogue converter to prevent the decoding of incorrect data. Additionally, fault-indication information is fed to an associated monitor unit[2].

The unit is constructed on a CH1/43A chassis with index-peg positions 1, 3 and 10. Power supplies at +12V, +5V and −12V are required.

## General Specification

*Inputs*

| | |
|---|---|
| Sync Fail | Normally logic level 1 (TTL), falling to logic 0 if syncs fail. This signal is an OR function of the outputs from the UN16/515 and UN16/517. |
| Word Valid | A positive-going signal from the digital-to-analogue converter indicating receipt of a valid word group. |
| Timing Generator Unlock | A signal (normally +12V) from the UN13/521 indicating that its a.f.c. system has locked the oscillator to the incoming syncs. |
| Video | A signal (nominally 2V p-p) from the AM18/521. |
| Sync Amplitude | A d.c. signal which corresponds to the bottom of syncs. |
| Pilot Tone Alarm | A signal which is derived from the UN3/27 and is normally at logic level 1 (TTL). The signal falls to logic 0 if the pilot tone is not within +2 dB or −20 dB of its nominal level. |
| Set | A signal from the MN1/7 which governs the operation of a timer circuit associated with the indicator lamps in the MN1/7. The signal is normally at logic 0 but rises to logic 1 for a short period following the clearance of a fault. |

*Outputs*

| | |
|---|---|
| Hold<br>Sync Fail<br>Pilot Tone<br>L.F. Overswing<br>Timing Generator Unlock | TTL signals which are at logic 0 in the absence of fault conditions. These signals are fed to the MN1/7 monitor. |
| Mute | A signal, normally at logic level 1 (TTL), which falls to logic 0 if the l.f. overswing, timing generator unlock or sync-fail circuits are activated. The mute pulse ceases about 2 ms after the last fault indication. |
| H.F. Overswing | A signal, normally at logic level 1 (TTL), which falls to logic 0 if overswings are present during the front-porch or sync-pulse periods. |
| Reset | A signal, normally at logic level 1 (TTL), which falls to logic 0 for 200 ns when the unit receives a *Set* pulse. |
| *TTL Logic Levels* | logic level 1, about +3·5V (+5V max.)<br>logic level 0, about 0V (+0·4V max.) |

## Circuit Description

A block diagram of the UN20/527 is given in Fig.1 and a circuit diagram in Fig.2.

*Overswing Detectors*

The video input signal is fed via emitter-followers TR1 and TR2 to an attenuator comprising resistors R6 and R7; the attenuated video is then fed to comparators IC2 and IC3.

The sync-amplitude input consists of a d.c. potential which corresponds to the bottom of syncs. This potential is attenuated by R8, R9 and R10, and is then applied as a reference potential (which is approximately 5 dB below sync bottoms) to comparator stage IC2 and inverter-amplifier IC1. The output of IC1 provides a reference potential which is approximately 5 dB above white level for use in comparator stage IC3.

For normal operation the outputs of comparators IC2 and IC3 are both at logic level 1, but any overswing which exceeds the reference limits (i.e. 5 dB below sync bottoms or 5 dB above white level) causes the output of the associated comparator to change to logic 0. The outputs of both comparators are fed via emitter-followers to IC4a; although IC4a is a NAND gate it provides an OR function if the circuit is considered as a whole, because either positive or negative overswings change the gate output from logic 0 to logic 1.

From IC4a the overswing information is fed to IC4b where it is applied to a NAND gate (pins 8, 9, 10) in conjunction with a pulse derived from a bistable stage in IC5. The pulse timings are such that any overswing occurring between the start of the front porch and the end of the sound-digit group will cause the *H.F. Overswing* output to change from logic 1 to logic 0.

When the output of IC4a changes state, C9 is charged via the 'pull-up' resistor in IC4b; the time constant is such that the output of gate 4,5,6 changes from logic 1 to logic 0 after about 10 $\mu$s. Thus an overswing occurring at any time which lasts for more than 10 $\mu$s causes the *L.f. overswing* output to change state and also operates the mute circuit.

*Timing Generator Unlock*

The timing-generator-unlock input signal is normally +12V, but it falls to below 6V for a fault indication. The signal is clipped by TR9, integrated and then fed via emitter-followers TR10 and TR11 to an inverter stage in IC7. From here the signal is fed to the muting circuit and it is fed also, via a further inverter in IC9a, to the Timing Generator Unlock output.

*Muting Circuit*

The three functions which can initiate a mute are:

Sync-fail
L.F. Overswing
Timing Generator Unlock.

All three functions are applied to gate 8,9,10,11 of IC7 at which point all are normally at logic level 1. Following a subsequent double inversion the mute output is taken from pin 6 of IC7 and is also normally logic 1.

When any of the three signals changes state, the mute output changes immediately to logic 0 and, because monostable stage IC8 is triggered also, a logic 0 is developed at pin 6 of IC8. (The monostable stage IC8 is a retriggerable device; unlike a conventional monostable multivibrator the timed state is commenced afresh by each input pulse so that, if the time interval between inputs is shorter than the time-constant of the circuit, the device remains in the timed state.) The output of the monostable remains at logic 0 for about 2 ms after the cessation of the input pulse (or pulses). Thus all mute signals originated by fault indication are widened by 2 ms, this gives the sync-separator and digit-separator units in the decoder time to recover after video disturbances.

*Output Logic*

The output signals on PLA pins 9,10,12,13 and 14 are all normally logic 0. Inverter stages IC9b, IC9c and IC9d, together with their associated diodes, prevent incorrect combinations of fault signals. For example, when syncs fail, the output of IC6d changes to logic 1 and the output of IC9b changes to logic 0. The IC9b output is applied via diodes D11, D12 and D13 to the *Hold, Pilot Tone* and *Timing Generator Unlock* outputs to prevent these from changing to logic 1. This action means that, in the steady state with no video input, the Decoder displays only the most important fault, i.e. *Sync Fail.*

Thus the following output combinations are possible:

*Sync Fail* (*Hold, Timing Generator Unlock* and *Pilot Tone* excluded)

*L.F. Overswing* (*Hold, Timing Generator Unlock* and *Pilot Tone* excluded)

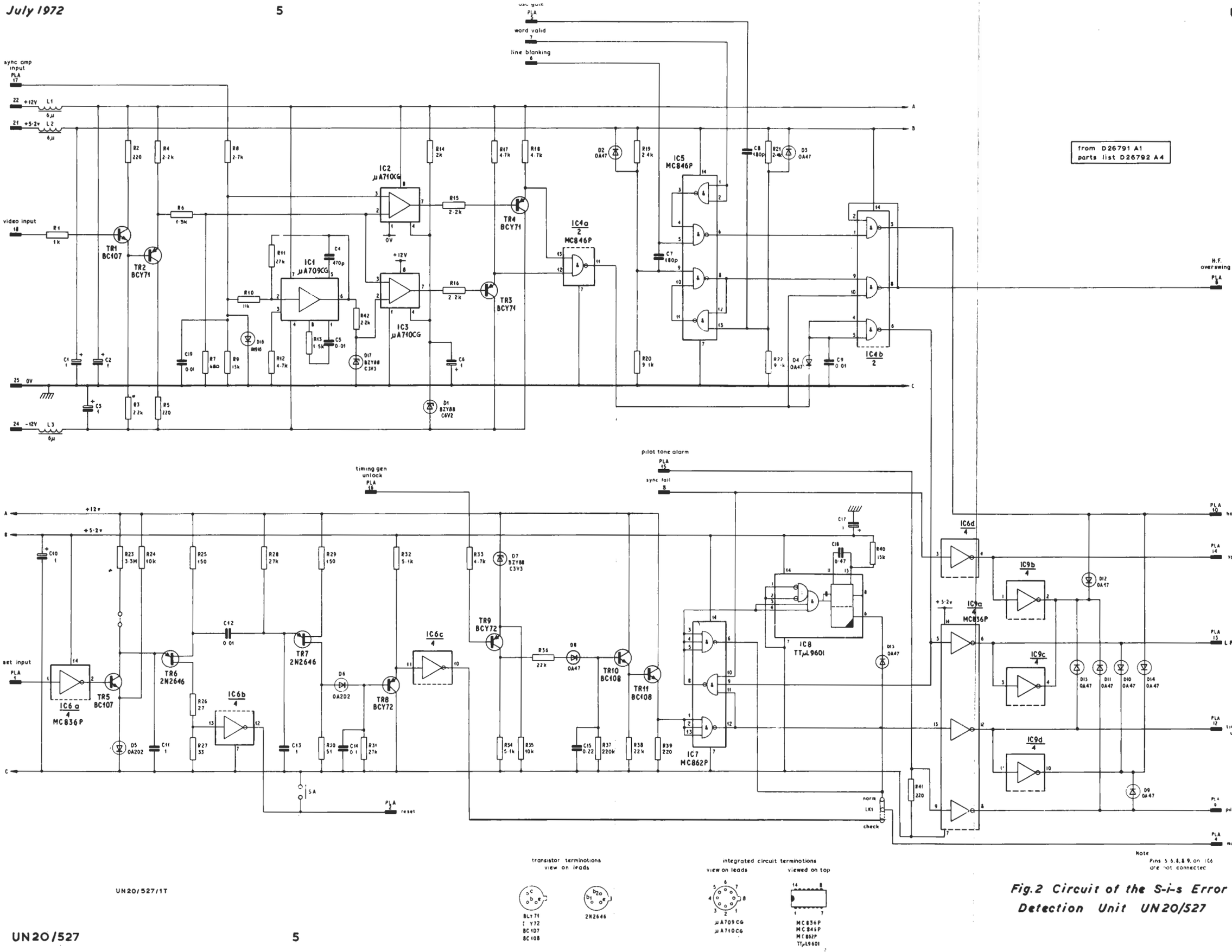
*Timing Generator Unlock* (*Hold, L.F. Overswing* and *Pilot Tone* excluded).

*Timer Circuits*

These circuits govern the operation of the lamps on the MN1/7 monitor. When a lamp is on but a fault signal is no longer present the *Set* input becomes a logic 1. This signal is fed via IC6a to TR5 which is cut off. Capacitor C11 commences to charge towards the +12V line via R23 and, when the potential across the capacitor reaches about 7V, uni-junction transistor TR6 conducts. Capacitor C11 discharges through TR6 and a positive-going pulse is applied to inverter stage IC6b the output of which is fed to the MN1/7 monitor to reset the indicator lamps. The lamps can be reset manually if required, by pressing push-button SA.

Unijunction transistor TR7 is a capacitor-discharge timer which functions in the same way as TR6. The output from TR7 is integrated and fed via TR8 to IC6c to provide a check-mute signal. The signal developed at pin 10 of IC6c normally has a value of logic 1 but falls to logic 0 for 5 ms once every 35 ms. The check-mute signal can be applied to the *Mute* output for test purposes by means of U-link LK1.

The negative-going edges produced at the emitter of TR7 each time C13 discharges are coupled via C12 to TR6 and are used to perform a strobe function. The




UN20/527/1T

transistor terminations view on leads

BCY71
BCY72
BC107
BC108

2N2646

integrated circuit terminations

view on leads

µA709CG
µA710CG

viewed on top

MC836P
MC846P
MC862P
TTµL9601

*Fig.2 Circuit of the S-i-s Error Detection Unit UN20/527*

purpose of this is to enable resistors of up to 20 megohms to be inserted in series with R23 so that the fault-indication lamps on the associated MN1/7 unit can remain illuminated for up to 20 seconds. The precise timing is decided by local operational requirements.

**Maintenance**

The UN20/527 forms part of a sound-in-syncs decoder and can be maintained only in conjunction with the other units of the decoder.

To check the operation of the unit:

1. Monitor the *Mute* output (PLA 4) with an oscilloscope probe. Remove the video input signal and check that the *Mute* output changes to logic 0.
   Press the *Reset* button. Observe the fault-indication lamps on the MN1/7 unit and check that only the *Alarm* and *Sync Fail* lamps are lit. Replace the video input.
2. Continue to monitor the *Mute* output. Place the UN23/531 unit on an extender board and use two fingers to bridge the cans of transistors TR4 and TR6. Check that the *Mute* output changes to logic 0 and that the *Timing Generator Unlock* lamp on the MN1/7 is illuminated.
   Replace the UN23/531 unit in the decoder.
3. Remove the UN23/525 unit. Observe the fault-indication lamps on the MN1/7 unit and check that the *Pilot Tone Alarm* lamp is illuminated.
   Replace the UN23/525 unit in the decoder.
4. Monitor the *Mute* output. Put U-link LK1 in the *Check* position. Observe the oscilloscope display and check that negative-going pulses with a duration of approximately 5·5 ms occur at intervals of 35 ms.

**References to Typical Associated Equipment**

1. Sound-in-syncs Decoder CD3M/504
2. Sound-in-syncs System Monitor MN1/7

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