SOUND-IN-SYNCS TIMING OSCILLATOR UN23/521

Introduction

The UN23/521 is used in the sound-in-syncs coders[1] and decoders[2] and, in conjunction with UN23/522 and UN23/523 units, produces all the pulse waveforms required for the operation of sound-in-syncs equipment.

Basically, the UN23/521 consists of a 10-MHz oscillator and a divide-by-640 counter. The oscillator starts within 50 ns when triggered by the leading edge of separated syncs and its output feeds the counter. The counter is never allowed to reach 640; when a count of 630 is reached (corresponding to a time of 63 μs) the oscillator stops and the counter is reset to zero. The oscillator is then retriggered by the leading edge of the next sync pulse.

The quiescent period of the oscillator is measured by an automatic-frequency-control circuit which ensures that the quiescent period is maintained at 1 μs; the maximum correction (or slew) rate is about 1 μs per second. The range of the automatic-frequency-control system is such that the unit can operate on line periods of 64 μs (−1, +1·5 μs).

The square-wave output of the counter effectively divides each line period into 50-ns intervals and thus the counter outputs provide information which enables any specific time slot in the line period to be located. These outputs (denoted A to K, L+63 and 2L+0·100) are fed to UN23/522 and UN23/523 units in which the required pulse chains for sound-in-syncs operation are derived. Note that the L+63 and 2L+0·100 designations refer to line frequency and twice-line frequency periods respectively, the figures represent an interval in microseconds timed from the leading edge of syncs.

The unit is constructed on a printed-wiring card; input and output connections are via an ISEP 33-way connector; index pin numbers are 3, 5 and 27. Power supplies at +12V, −12V, +5·2V and −5·2V are required.

General Specification

*Inputs**

Syncs	positive-going separated mixed sync or line-drive pulses at TTL logic level 1.
1-μs Pulse	positive-going pulse coincident with leading edge of syncs, duration 1 μs, TTL logic level 1.

Outputs

Counter Outputs	pulse outputs taken from each stage of the divide-by-640 counter and denoted A to K. (A to J are MECL logic k is TTL logic)
Stop Pulse	produced when the count reaches 630 and denoted L + 63, MECL logic levels.
2L + 0·100	a twice line rate negative-going pulse, TTL logic levels
Oscillator Unlocked	an alarm signal indicating that the oscillator is not locked to incoming sync pulses.

Power Requirements	60 mA at +12V, 60 mA at −12V. 12 mA at +5·2, 350 mA at −5·2V

Logic Levels

TTL Levels	logic level 1, about +3·5V (+4V max.) logic level 0, about 0V (0·4V max)
MECL levels	logic level 1, about −0·75V (−0·7V max.) logic level 0, about −1·75V (−1·5V max.)

Circuit Description

A circuit diagram of the UN23/521 is given in Fig.1 and waveforms are given in Figs.2 and 3. The operation of the circuit is described below from the receipt of one sync pulse to the arrival of the next.

*Normally obtained from a UN16/514 or UN16/515 unit.

Continued Overleaf

Start Circuit

Positive-going separated syncs at TTL logic level 1 are applied to PLA 28. Because the input logic of the circuit is MECL the resistors R9, R13 and R14 are provided to translate the 4V p-p incoming syncs to MECL levels; i.e. −1·5V to −0·7V. The leading edge of each sync pulse triggers an RS bistable contained in IC17 (pins 8 to 13) and the resulting change of state cuts off the TR4 side of the long-tailed pair formed by transistors TR4 and TR5.

Oscillator

Immediately before the arrival of a sync pulse, transistor TR3 is cut off and capacitor C5 is charged to the potential at the junction of R19 and R20 (+1·3V). The arrival of the leading edge of the sync pulse cuts off TR4, whereupon transistor TR3 turns on and C5 commences to discharge through L1. Thus the first cycle of oscillation is started by energy stored in the capacitor. (Varactor diode D2 forms part of the a.f.c. circuit and is described later.) The output of the oscillator is fed via emitter-follower TR1 to the logic stages contained in IC11; the frequency is 10 MHz and the signal amplitude at this point is about 4V peak-to-peak.

Clock Squarer

The 10-MHz sine wave fed to IC11 is gated with the start signal derived from pin 11 of IC17 and squared. Resistor R1 provides bias to define the d.c. level of the sine wave and so ensure symmetrical disposition of the waveform between logic levels 1 and 0. The state of the gates contained in IC11, for both positive and negative half-cycles of the clock pulses, are shown in Table 1.

TABLE 1

Pin 1 (start signal)	*Pins 2 and 4 (osc. output)*	*Pins 3 and 10* –	*Pins 5 and 2 (clock)*	*Pins 6 and 9 (invert. clock)*
0	+ve	0	1	0
0	−ve	1	0	1

Counter

(a) Divider Stages

The counter format is given below:

IC1 to IC4 form a divide-by-16 stage
IC5 forms a divide-by-2 stage
IC6 to IC9 form a divide-by-10 stage
IC10 forms a divide-by-2 stage

At the start of a counting sequence (i.e. after a reset) all the Q (pin 13) outputs of the counter are at logic 0 and all the Q (pin 1) outputs are at logic 1.

Unused inputs on the counter gates are connected to −5V (to obtain maximum operating speed and reduce interference effects).

The counter is capable of dividing by 640 (i.e. 16 x 2 x 10 x 2) but the count is stopped at 630 by means of IC16. Integrated circuit IC16 functions as a NOR gate and is fed from the $\overline{Q}$ outputs of IC2, IC3, IC5, IC6, IC9 and IC10. The states of the individual counter stages when the count reaches 630 are shown in Table 2. If the table is compared with the circuit diagram (Fig.1) it can be seen that the inputs to IC16 are the complement of the binary number 630; i.e. they are the $\overline{Q}$ outputs of those stages that produce a logic 1 at their Q outputs for a count of 630.

TABLE 2

Binary Weighting	IC Number	Q Output for Count of 630
1	IC1	0
2	IC2	1
4	IC3	1
8	IC4	0
16	IC5	1
32	IC6	1
64	IC7	0
128	IC8	0
256	IC9	1
320	IC10	1

(b) Counter Reset

When all the inputs to IC16 are at logic 0 the output changes to logic 1 and a reset pulse is applied to the RS bistable stage defined by pins 8 to 13 of IC17. The output of this bistable stops the clock-pulse generator by applying a logic 0 to pins 12 and 13 of IC11 and stops the oscillator as well by changing the state of the long-tailed pair TR4-TR5. The logic 1 present at pin 8 of IC17 is used to reset the counter in preparation for the next count.

(c) Counter Outputs

Pulses A to J are taken from the Q (pin 13) outputs of the appropriate stages of the counter and are then fed to A to J outputs of the unit via NOR gates which provide a negative-going output.

The Q and $\overline{Q}$ outputs of IC10 feed a long-tailed pair comprising transistors TR16 and TR17; the K output

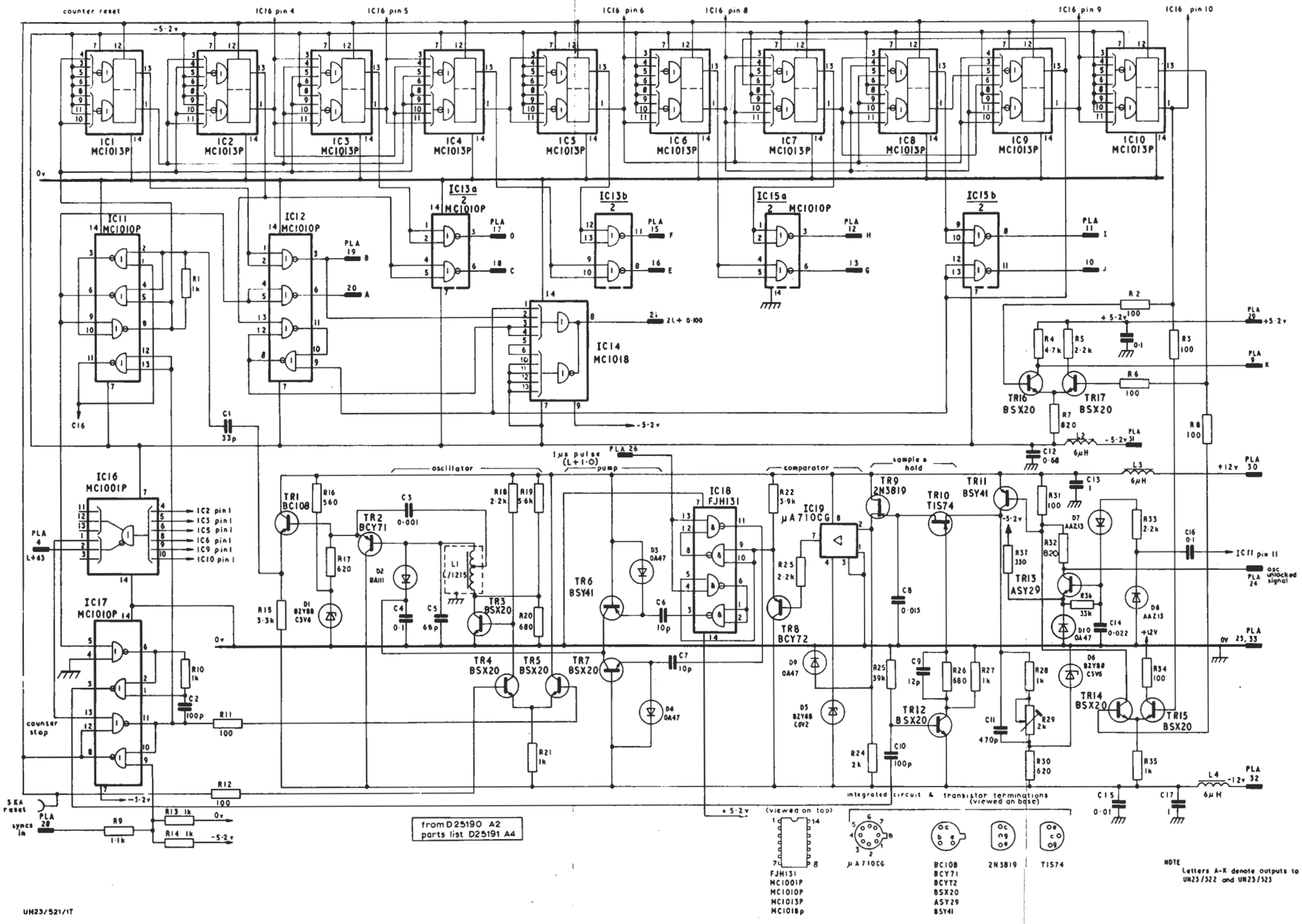


Fig.1 Circuit of the S.i.s. Timing Oscillator UN23/521

is taken from the collector of TR16. The purpose of the long-tailed pair is to convert the MECL output of IC10 to TTL levels.

(d) 2L +0·100

Waveforms associated with the generation of the 2L+0·100 output are shown in Fig.3(a) and the circuit is described below.

Integrated circuit IC14 is a MECL to TTL converter which can be used either as a four-input OR gate or as a five-input NOR gate. In this instance the OR gate is used and the NOR gate is rendered inoperative by the connection of pin 6 to the reference-bias point (pin 5). A negative-going output is required and this occurs twice in each line period; the first time is 100 ns after the leading edge of syncs when the B output of the counter first changes from logic 1 to logic 0 (see waveforms) and the second time is when a count of 321 has been reached (i.e. the first time that the B output changes state following a K output).

Note that the output of IC14 does not have an active 'pull-up' stage and hence the trailing edge of the 2L +0·100 waveform takes approximately 300 ns to recover.

Automatic Frequency Control

(a) Exponential Voltage Generator

The Q and $\overline{Q}$ outputs of the last stage (IC10) of the counter are applied to the long-tailed pair comprising transistors TR14 and TR15. After a count of 320 the Q (pin 13) output of IC10 is at logic 1; thus TR14 is turned on and TR15 cut off. The change of potential at the collector of TR14 turns on TR11 and capacitor C11 commences to charge towards +12V. When the counter reaches a count of 630 the Q output of IC10 changes to logic 0 with the result that TR14 cuts off and TR15 turns on. When TR14 cuts off, TR11 cuts off also and capacitor C11 discharges exponentially, through R28 and R29, towards a potential of −5·6V which is set by D6. The discharge time-constant is determined by the setting of R29.

(b) Sample and Hold

The sample-and-hold waveforms are shown in Fig.3(b) and the circuit is described below.

One microsecond after a count of 630 has been reached, the leading edge of the following sync pulse arrives at the input to the unit and causes the RS bistable stage formed by pins 8 to 13 of IC17 to change state, whereupon the logic level on pin 11 changes from 0 to 1. The leading edge of the transition on pin 11 is coupled via C2 to another RS bistable stage which is formed by pins 1 to 6 of IC17. This stage is subsequently reset by the leading edge of the first 10-MHz clock pulse; the narrow negative-going pulse which is developed at pin 3 of IC17 is used to cut TR12 off and hence turn TR10 on. Transistor TR10 acts as a switch and during the period for which it is turned on the exponential waveform present at the collector of TR11 is sampled and stored in C8. The potential developed across C8 is applied via source-follower TR9 to integrated circuit IC19; TR9 has a high input impedance and so it does not materially discharge C8. The offset potential of TR9 is such that in normal operation its input (i.e. C8) is at approximately −1V and its output at 0V.

(c) Comparator

Integrated circuit IC19 compares the output of TR9 (applied to pin 2) with a 0V reference potential which is applied to pin 3. If the voltage on pin 2 is higher than 0V the output of the comparator is high and if the voltage on pin 2 is lower than 0V the output of the comparator is low. The comparator output is changed to the appropriate logic level by emitter-follower TR8 and is then fed to pins 9, 10 and 5 of integrated circuit IC18. Integrated circuit IC18 is fed also with a pulse which occurs 1 μs after the leading edge of syncs and is thus time-coincident with the comparator output. The logic of IC18 is such that when the comparator output is high a negative-going pulse is fed via C7 to TR7; conversely, when the comparator output is low, a positive-going pulse is fed via C6 to TR6.

(d) Pump Circuit

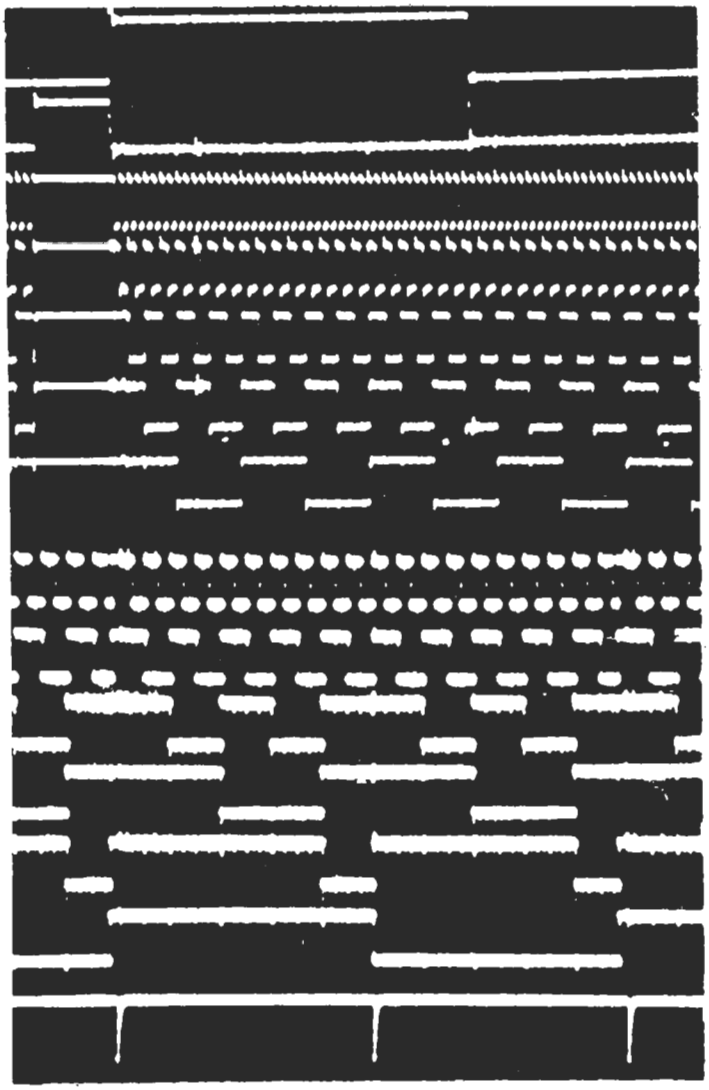
The frequency of the oscillator is adjusted by varying the reverse bias which is applied to varactor diode D2 by capacitor C4. The action of the circuit is described below.

Transistors TR6 and TR7 are both normally turned off, because their bases and emitters are at the same potential. When a positive-going pulse is applied via C6 to TR6 the emitter of TR6 becomes momentarily more positive than its base. Thus the transistor conducts and the potential across capacitor C4 is increased. A similar action takes place when a negative-going pulse is fed via C7 to the emitter of TR7, but the result in this instance is that the potential of C4 is reduced. The values of C6 and C7 are only 10 pF but the value of C4 is 0·1 μF; therefore the change in the potential of C4 caused by a single pump action is very small and the oscillator is steered into lock by incremental line-by-line adjustments to the potential across C4.

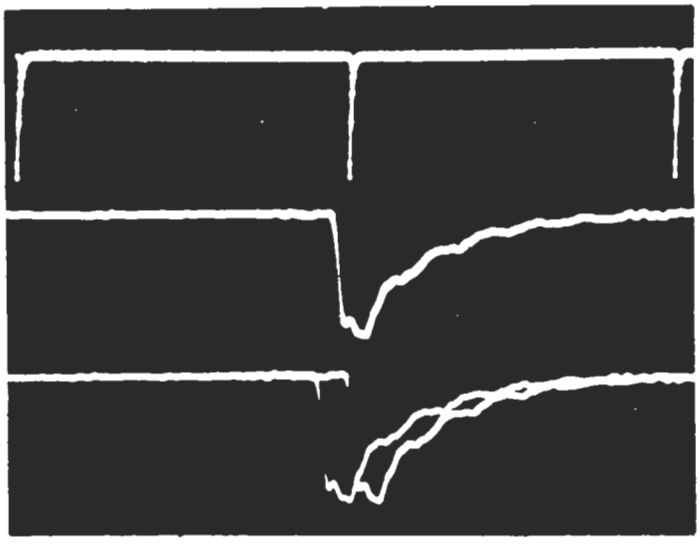
Once the oscillator is locked the pump action continues and alternates between the charge and discharge conditions. Transistors TR6 and TR7 tend to conduct for a few lines each with the result that a jitter of about ±10 ns is produced on the count period of 63 μs.

(e) Starting Conditions–The Action of TR13

When the unit is first powered, the potential on C4 is 0V and the oscillator runs at too low a frequency. The counter takes about 1·25 lines to reach a count of 630; thus the counter-reset pulses last for about 40 μs and the oscillator triggers, in effect, on alternate lines. To bring the oscillator into lock as rapidly as possible the exponential waveform developed across C11 is inhibited at the end of the first count and the collector of TR11 is held at +12V by the action of a d.c. restorer and integrator (comprising C16, C14, R33, D7, D8 and TR13) which is driven by the extra-long reset pulses. As a result, pump pulses are fed exclusively to TR6 and the potential on C4 is raised rapidly to the correct



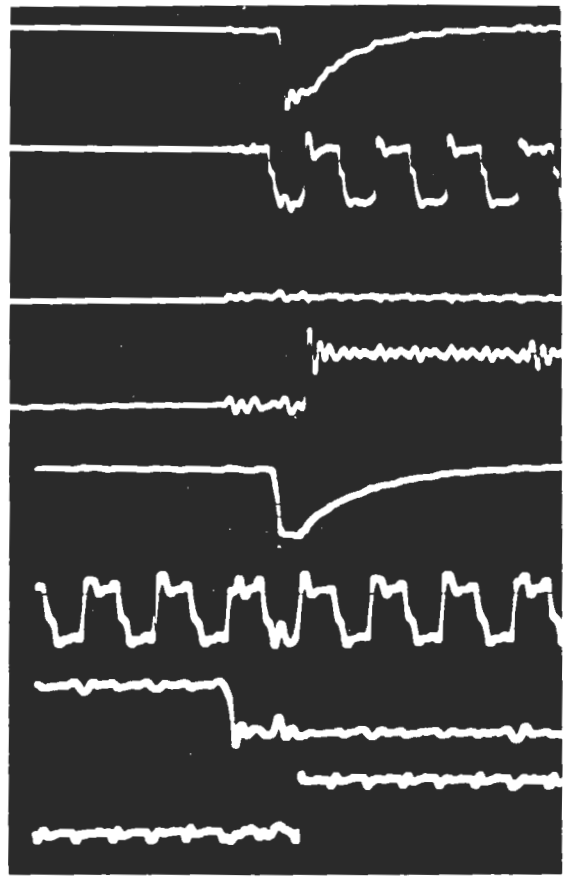
(a) Output Waveforms



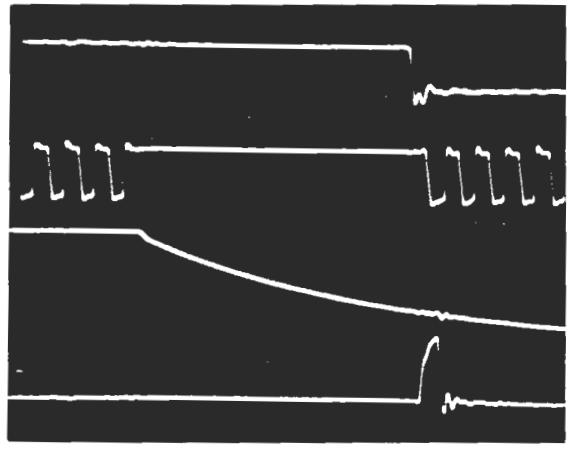
(b) Adjustment of R29

UN23/521/2P

Fig.2 Waveforms in the UN23/521



(a) Generation of 2L+0·100



(b) Sample and Hold Waveforms
(Sep Syncs and A waveforms included as timing references)

UN23/521/3P

Fig.3 Waveforms in the UN23/521

operating point (about +3V).

When the oscillator is locked and the counter is producing 1-μs reset pulses, only a small amount of energy is applied to the integrator and TR13 remains cut off. The collector of TR13 is connected to PLA 24 and thus an alarm signal is provided when the oscillator is not locked to the incoming sync pulses.

Maintenance

The following points may assist in maintenance:

1. Almost all fault conditions result in the 1-μs reset pulse (available at SKA) being either absent or of incorrect duration.
2. If faults in the a.f.c. system are difficult to locate, connect the cathode of D2 to the +5V line. The duration of the reset pulse can then be set by adjusting the core of L1; when the pulse duration is less than 1μs the potential at the collectors of TR6 and TR7 should be about +12V, when the pulse duration is greater than 1μs the collector potential should be about 0V.
3. If the reset pulse apparently locks at 1μs but the 2L +0·100 pulses are incorrectly positioned, the fault is probably caused by the counter not dividing by 630. A faulty counter stage can be readily located by comparing the counter outputs with the waveforms given in Fig.2 (a).

Test Procedure

To test the UN23/521 proceed as follows:

1. Attach the unit to an extender board and insert the combination into a working sound-in-syncs coder or decoder.
2. Feed the equipment with a Network video signal (this is necessary because the output of self-contained test-waveform generators may not provide a line period which is accurately maintained at 64μs.). Using an oscilloscope, monitor and reset pulses present at SKA and check that they are approximately 1μs in duration.
3. Introduce an error into the a.f.c. system by bridging the cans of TR6 and TR5 with moist fingers (this simulates the Unlocked–Fast condition). If the a.f.c. system is working correctly, the potential on C4 should increase to about +12V and the duration of the reset pulses should increase.
   Remove the fingers and check that the reset pulses return to the 1-μs Locked condition within about 2 seconds.
4. Introduce a different error into the a.f.c. system by using moist fingers to bridge the cans of both TR6 and TR7 to the can of TR4 (this simulates the Unlocked–Slow condition). If the a.f.c. system is working correctly the duration of the reset pulses should first decrease; longer pulses should then occur on alternate lines.
   Remove the fingers and check that the reset pulses return to the 1-μs Locked condition.
5. Set the oscilloscope for d.c. measurement and use a probe to check that the potential on the collectors of TR6 and TR7 is +3·5V. If it is not, adjust the core of L3 until the correct reading is obtained. Note that the junction of TR6 and TR7 is a point of very high impedance; therefore the measurement should be made by momentarily touching the collector (the can of either TR6 or TR7) with the probe, because fastening the probe to the measurement point will result in undue loading.
6. Monitor the 2L +0·100 pulse which is present at PLA 21. Set the oscilloscope to trigger on INT –VE and adjust the time base so that 3 pulses are displayed, as shown in Fig.2(b).
   Expand the trace and examine the centre pulse. If what appears to be the centre pulse is seen to consist of two separate pulses, adjust R29 until the two pulses become coincident. (This adjustment effectively sets the duration of the 1-μs pulse by ensuring that the 2L +0·100 pulse produced in the middle of each line occurs at precisely L +32·1μs.)

References to Typical Associated Equipment

1. Sound-in-syncs Coder CD2M/505
2. Sound-in-syncs Decoder CD3M/504

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