S.I.S. TIMING GATES LOGIC UNIT UN23/523

Introduction

The UN23/523 is used, in conjunction with a UN23/521 Timing Oscillator, to produce a number of pulse waveforms for use in sound-in-syncs decoders [1]. The unit accepts the outputs of the counters contained in the UN23/521 and, by means of logic gating processes, produces six outputs which are accurately timed with respect to the input signals.

The unit is constructed on a printed-wiring card fitted with a 33-way ISEP connector. Index-pin positions are 3, 17 and 27. Power supplies at +5V and −5V are required.

General Specification

The labels given to signals in the Specification refer to timings, measured from the leading edge of syncs, of line-frequency or twice-line-frequency waveforms (L or 2L).

Inputs	A to K, MECL logic 2L + 0·100, TTL logic L + 63, MECL logic
Outputs (at TTL levels)	Line Blanking, (L + 63) to (L + 9·9) Marker Detect, (L + 0·100 to (L + 0·55) Transfer Gates, (2L + 5·6) Counter Start, (2L + 9·4) Equalising-pulse Interrogate, (L + 32·8) to (L + 33·6) Sync Gate, (L + 63) to (L + 5·2)
Power Consumption	40 mA at +5·2V, 150 mA at −5·2V
Logic Levels	
TTL	logic level 1, about +3·5V (+5V max.) logic level 0, about 0V, (+0·4V max.)
MECL	logic level 1, about −0·75V (−0·7V max.) logic level 0, about −1·75V (−1·5V max).

Continued overleaf

Circuit Description

A circuit diagram is shown in Fig. 1 and the output waveforms obtained for normal working conditions are given in Fig. 2.

General

All the pulses produced by the UN23/523 are derived by gating the correct combination of waveforms from the UN23/521. These input waveforms are derived from a 10-MHz oscillator in the UN23/521 which is locked to the leading edge of syncs. Thus all the waveforms produced by the UN23/523 are static with respect to syncs. Input waveforms B to J consist of successive divisions of the basic 10-MHz signal (waveform A); input K changes state 32 μs after the leading edge of syncs and again at 63 μs; the other two input waveforms are defined by their titles. By gating the appropriate waveforms a pulse can be generated in any specific 50-nanosecond time-slot in the line period.

The pulses produced by the UN23/523 fall into two groups: those in one group are defined in terms of position and duration, but those in the other group are defined in terms of position only. Where pulses of defined position and duration are required (e.g. line-blanking or sync-gate pulses) they are generated by bistable circuits. However, where pulse position is the sole criterion and only one edge is required (e.g. to initiate an operation in an analogue-to-digital converter) the appropriate pulse can be generated in a single logic gate which ensures that the leading edge occurs at the correct time; the pulse duration is fixed but is not important.

Circuit Details

(a) Line Blanking

The bistable stage formed by IC3 (pins 8 to 13) is set by the (L + 63) pulse and is reset by a pulse occurring 9·9 μs after the leading edge of line syncs which is derived from IC2 (pins 1 to 4). The line-blanking pulse developed at the output of the bistable stage (pin 8) is in MECL levels and is applied to a NOR gate in IC10 which translates the signal to TTL levels.

(b) Marker Detect

The bistable stage contained in IC4 is set by alternate (2L + 0·100) pulses and reset at (L + 0·55) by the first negative-going pulse in each line period which is provided by IC5. The application of a $\overline{K}$ pulse to pin 10 of IC4 prevents the operation of the bistable stage being upset by the half-line (2L + 0·100) pulses.

(c) Transfer Gates

Integrated circuit IC6 contains a NOR gate which is used both to derive this pulse and to translate it to TTL levels. The pulse duration is the duration of the E-input pulse; i.e. 0·8 μs.

(d) Counter Start

This pulse is derived from IC7 where the two gates contained in the integrated circuit are combined to provide a 7-input NOR gate. The output is kept in MECL form because it is required to feed MECL logic circuits in the UN23/526 Counter Logic Unit.

Equalising Pulse Interrogate

This pulse is formed in a NOR gate contained in IC8; it is used in the UN23/529 Sync Regenerator unit, in conjunction with separated sync pulses, to locate the first half-line equalising pulse in the video waveform.

Sync Gate

The bistable stage formed by pins 8 to 13 of IC11 is set by the leading edge of line blanking which is coupled via C3 to pin 13. The reset pulse is derived from IC9 which produces positive-going 2L + 5·6 pulses with a duration of 0·4 μs. These pulses are gated with $\overline{K}$ pulses in IC11 (pins 4 to 6) to produce a line-rate output at L+5·6 which is applied to pin 9 of IC11 as a reset pulse.

Maintenance

Generally, faults in the logic circuits cause either the loss of one or more outputs or result in an output being drastically altered; for example a faulty marker-detect output might contain two pulses per line mistimed and so rapid fault diagnosis can be made by comparing the outputs with the waveforms shown in Fig. 2.

The loss of one or more outputs can often be traced to a common fault; for example if the (L + 63) pulse is absent the line-blanking and sync-blanking outputs will be lost.

Permanent faults in integrated circuits are usually of a catastrophic nature; for example a faulty gate might have an output that is permanently set to logic 1, logic 0 or some intermediate value, regardless of input conditions. Intermittent faults are generally caused by dry joints or by hair-line cracks in the copper track. Faults of this type are often revealed by a thorough mechanical inspection.

When the UN23/523 is placed on an extender board the line-blanking and sync-gate outputs may be lost. This is caused by cross-talk and earth-loop effects upsetting the operation of IC2. To overcome this difficulty, connect the earth at the top of the printed-wiring card to the decoder chassis by means of a short crocodile-clip lead. When using an oscilloscope probe to check logic funtions make sure that the probe earth clip is connected to the earth line of the unit.

References to Typical Associated Equipment

1. Sound-in-syncs Decoder CD3M/504

TES 6/71.

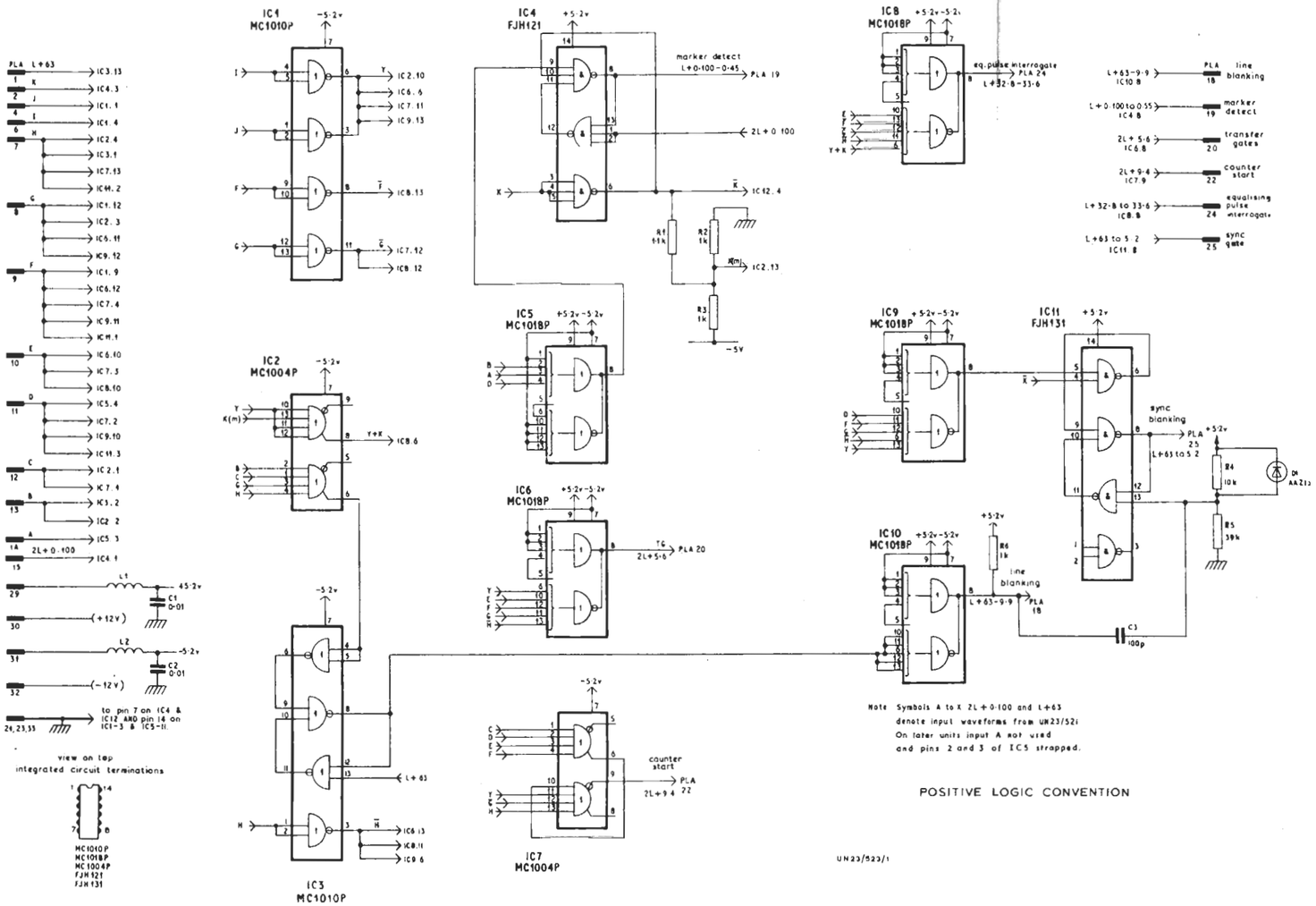

Fig. 1 Circuit of the Timing-gates Logic Unit UN23/523

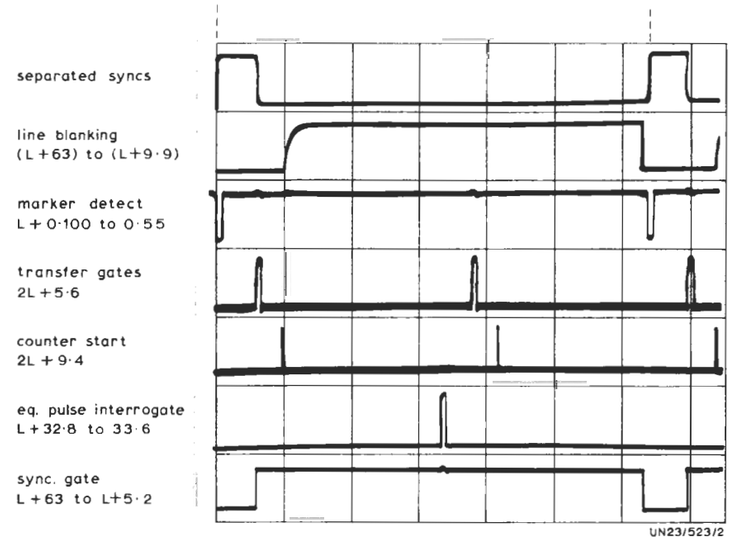

Fig. 2 Waveforms in the Logic Unit