SOUND IN SYNCS SHIFT REGISTER UN23/524

Introduction

The UN23/524, a 22-bit shift register with serial input and parallel output, forms part of a sound-in-syncs decoder[1]. The unit accepts a 21-bit sound-in-syncs combined pulse group from which it derives two 10-bit coded words. When the words have been read-out the register is reset in preparation for the next operating cycle.

The 21-bit input signal is read into the register until the first bit (a marker pulse) reaches the end of the register when the process is stopped. The contents of the register are then inspected to verify:

(a) that the marker pulse is present;

(b) that a spurious 22nd bit is not present.

If either (a) or (b) is incorrect an error signal is generated and the contents of the register are not used in subsequent units of the decoder.

The UN23/524 is constructed on a printed-wiring card fitted with a 33-way ISEP connector. Index-pin positions are 3, 5 and 21. A 5-volt power supply is required.

General Specification

Input Signals

Digit Input	line-repetitive, negative-going pulse train (obtained from UN16/517)
Reset Input	line-repetitive, negative-going pulse, starting 59·3μs after the leading edge of syncs (obtained from UN23/523)
Shift Input	line-repetitive train of 22 negative-going pulses, repetition period 182 ns, nominal pulse duration 50 ns (obtained from UN23/531).
Transfer Odd Input	line-repetitive positive-going pulse, starting 37·6μs after the leading edge of syncs (obtained from UN23/525).
Transfer Even Input	line-repetitive positive-going pulse, starting 5·6μs after the leading edge of syncs (obtained from UN23/525).
H.F. Overswing Input	logic level 1, unless an overswing is present (obtained from UN20/527).
Marker Detect Input	line-repetitive negative-going pulse

Output Signals

Digit Outputs	ten separate outputs, one for each bit of the ten-bit coded word, labelled d1 to d10.
Shift Start Output	line-repetitive positive-going pulse, present when the marker pulse coincides with the marker-detect input.
Shift Stop Output	line-repetitive negative-going pulse, generated when the digit input signal has been transferred to the register.
Word Valid Output	line-repetitive pulse, negative-going at start of input sequence but changing to positive-going (see text) unless the input signal is faulty.

Power Requirements 370 mA at +5V.

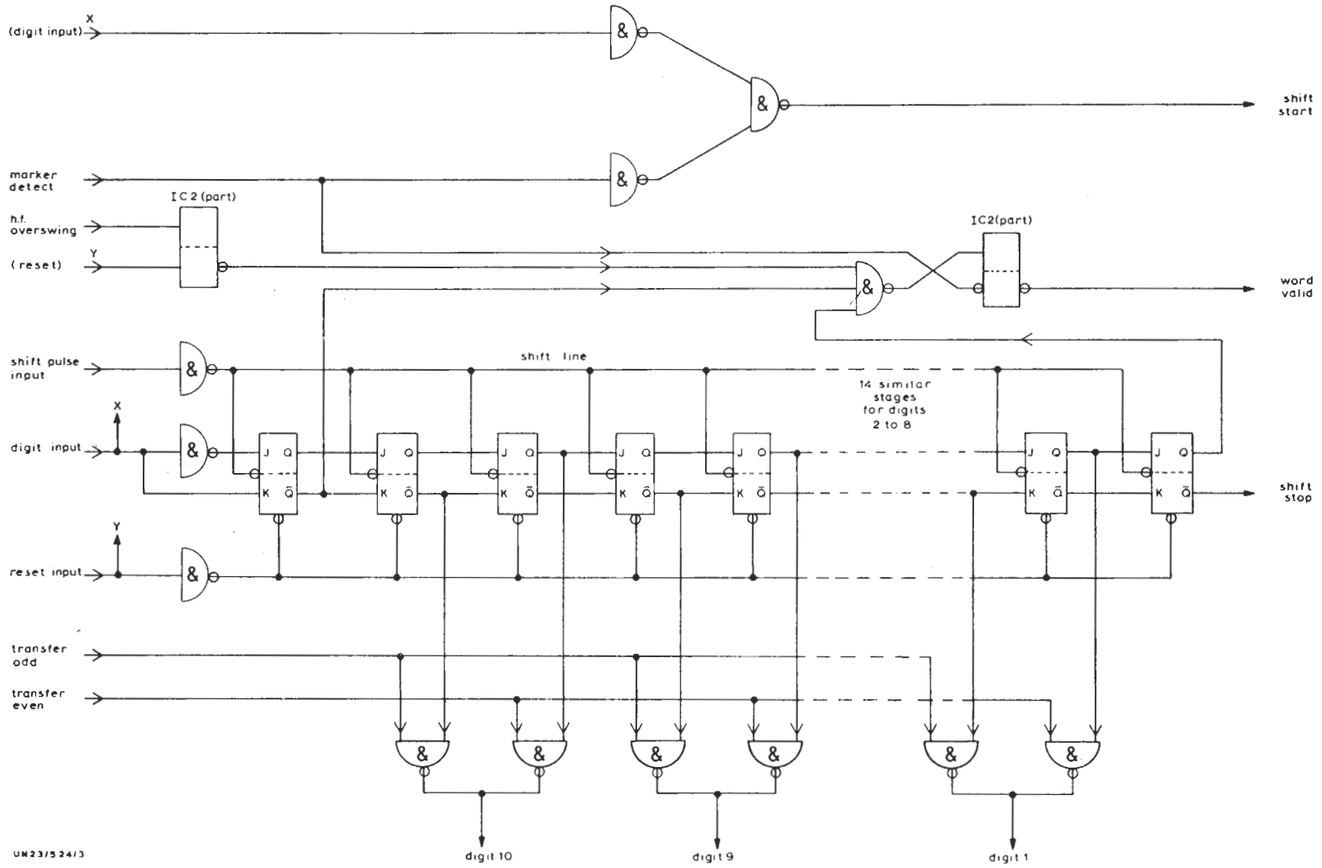


Fig. 1 Simplified Logic Diagram of the UN23/524

Note: All inputs and outputs are TTL logic signals.
TTL logic levels are:
logic level 1, about +3·5V (+5V max.)
logic level 0, about 0V (+0·4V max.)

Circuit Description

A simplified logic diagram of the UN23/524 is given in Fig.1 and a detailed circuit diagram in Fig.2.

The shift register consists of 22 JK bistable stages IC5 to IC10 and IC14 to IC18 (see Instruction GP.1) and is initially set up so that the Q output of each stage is at logic 0. The sound-in-syncs combined pulse group (labelled digit input in the circuit) is fed directly to the K input of the first bistable stage and via an inverter to the J input. Before the signal can be read into the register a shift-start pulse must be generated; this pulse is generated by NAND gate which is fed with an inverted feed of the digit input signal and an inverted marker-detect pulse; if these two pulses occur at the same time a logic 0 is developed at the shift-start output. The leading edge of this shift-start pulse is used in an associated sample-and-hold unit[2] to initiate shift pulses which, when fed back to the UN23/524, cause the digit input signal to be read into the register. The delay involved in producing shift pulses is such that the first shift pulse starts at about the mid-point of the marker pulse. When the marker pulse reaches the end of the register, the $\overline{Q}$ output of IC18b changes to logic 0; this change is used to prevent the production of further shift pulses.

After all 21 pulses of the digit input signal have been read into the register its contents are examined to verify the presence of a marker pulse and the absence of a spurious pulse in the 22nd-bit position. The results of these two checks are fed to a NAND gate, together with information regarding the presence or absence of an overswing (a voltage overswing on the combined sound-in-syncs signal of more than 5 dB above peak white or more than 5 dB below sync bottoms). If all three inputs to the gate are at logic level 1, (the no-faults condition) a logic 0 is applied to an RS bistable stage formed by part of IC2, and a logic 1 is developed and fed to the *word-valid* output.

At the end of the reading-in process, the register contains two interleaved and complemented ten-bit words plus a marker pulse. The first ten-bit word is held in stages IC6a, IC7a, IC8a, and so on; the complemented second word is held in stages IC5b, IC6b, IC7b, and so on. The least significant bits follow the marker pulse and thus are held in stages IC17b and IC18a. Transfer pulses are used to extract the two ten-bit words from the register. When the *transfer even* line is at logic 1, the NAND gates associated with the digits of the first word are opened and the digits are read at the appropriate outputs. When the *transfer odd* line is at logic 1 the gates associated with the second word are opened and the digits of the second word are read out.

Because the second word is complemented when it forms part of the sound-in-syncs signal, the digits of the second word are taken from the $\overline{Q}$ outputs of the register where the word is held in its correct form. Note that both the stored words are subsequently inverted by the action of the output gates and so a further inversion is needed in the following unit[4] to restore them to their correct form.

When the reading-out process has been completed, all stages of the shift register are reset to the Q = 0 condition in preparation for the arrival of the next combined pulse group.

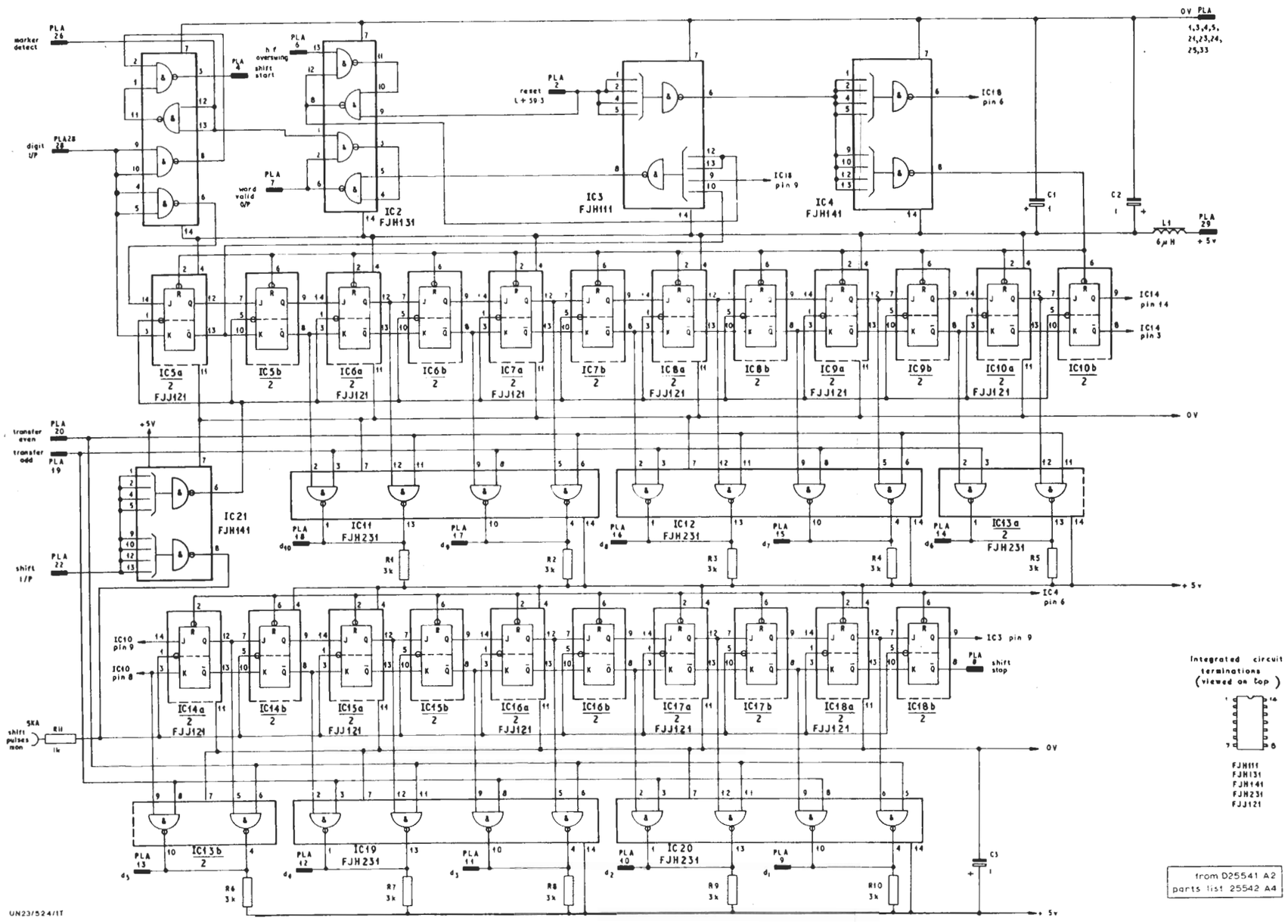
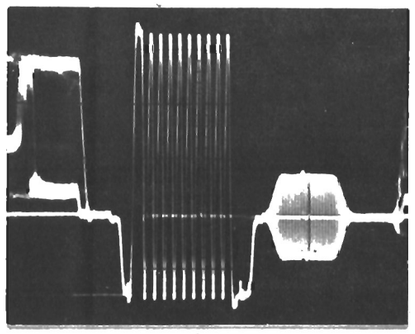
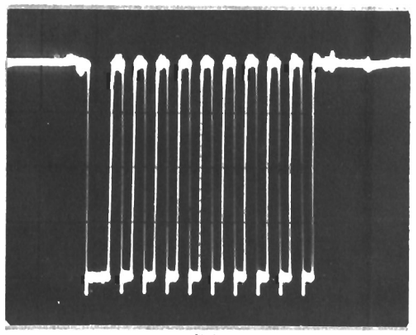


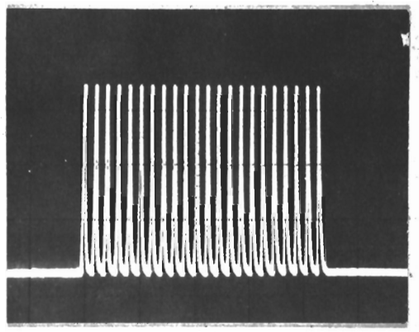
Fig.2 Circuit of the S.i.s. Shift Register UN23/524



(a)

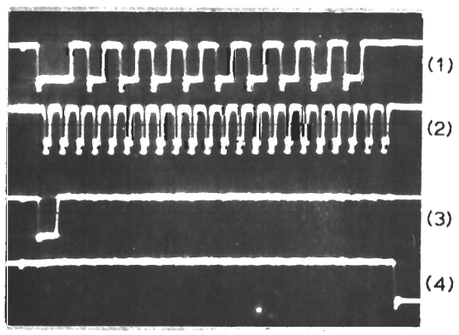


(b)

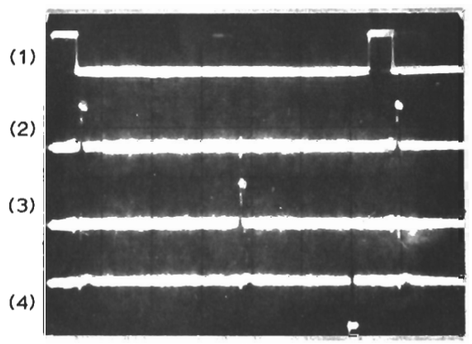


(c)

UN23/524/2P



(d)



(e)

Fig. 3 Waveforms in the UN23/524

(a) s.i.s. full count waveform
(b) digit input about 4V p-p
(c) shift pulses about 3V p-p
(d) relative timing of (1) digit input (2) shift input (3) shift start (4) shift stop; all at 0·5 μs/div
(e) relative timing of (1) sep syncs from UN16/515 (2) transfer even (3) transfer odd (4) reset; all at 10 μs/div.

Maintenance

To check the operation of the unit:

1. Apply a full-count sound-in-syncs signal to the input of the parent decoder. (This signal is shown in Fig.3a and can be produced by removing the UN23/528 unit from the associated coder[3].)
2. Check that the *Digit* and *Shift Pulse* inputs are as shown in Figs.3b and 3c respectively. If the shift pulses are missing, check that a *Shift Start* pulse is present at PLA 4. If the shift pulses are continuous, check that a *Shift Stop* pulse is present at PLA 8 when the reading-in process has been completed.
3. Check the digit outputs *d1* to *d10* in turn. Negative-going pulses at twice line rate should be present. Check that the pulse timings with respect to the leading edge of syncs are +5·6μs and +37·6μs. If either the odd or even sets of digit outputs are missing, check the transfer pulse inputs on PLA 19 and PLA 20.

References to Typical Associated Equipment

1. Sound-in-syncs Decoder CD3M/504.
2. Sample and Hold Unit UN23/531.
3. Sound-in-syncs Coder CD2M/505.
4. Sound-in-syncs Gated Staticiser Unit UN23/525.