SOUND IN SYNCS COUNTER AND LOGIC UNIT UN23/526

Introduction

The UN23/526 is a ten-stage ripple-through binary down-counter (see Instruction GP.1) which operates at a clock frequency of 50 MHz and forms part of a sound-in-syncs decoder[1]. In conjunction with the associated sample-and-hold unit the UN23/526 converts digital information to analogue form.

The ten stages of the counter accept a 10-bit coded word and, on the receipt of a counter-start command signal, the counter counts downwards to zero. At the start of the count the unit provides a *Ramp Start* output which is fed to a ramp generator in an associated sample-and-hold unit[2]; when the count reaches zero a *Ramp Hold* output is fed to the ramp generator.

The UN23/526 is constructed on a printed-wiring card fitted with a 33-way ISEP connector. Index-pin positions are 3, 5 and 25. Power supplies at −12 volts and −5 volts are required.

General Specification

Inputs

Counter Inputs	ten inputs, one for each bit of the coded word, labelled *d1* to *d10*, TTL logic (obtained from UN23/525)
Counter Start	positive-going pulses at twice line rate delayed by 9·4μs w.r.t. the leading edge of syncs (2L+9·4); MECL logic (obtained from UN23/523)
2L + 4·8 Input	positive-going pulses at twice line rate, TTL logic (obtained from UN23/522)

Outputs

Ramp Hold	positive-going pulses at twice line rate, MECL logic.
Ramp Start	positive-going pulses at twice line rate, MECL logic

Power Requirements 9 mA at −12V, 45 mA at −5V.

Logic Levels

TTL levels	logic level 1, about +3·5V (+5V max.) logic level 0, about 0V (+0·4V max.)
MECL levels	logic level 1, about −0·75V (−0·7V max.) logic level 0, about −1·75V (−1·5V max.)

Circuit Description

A simplified block diagram of the UN23/526 is shown in Fig.1 and a detailed circuit diagram in Fig.2.

The counter consists of 10 JK bistable devices IC17 and 1IC1 to 9IC1 (see Instruction GP.1) which are connected as a ripple-through down-counter; i.e. a

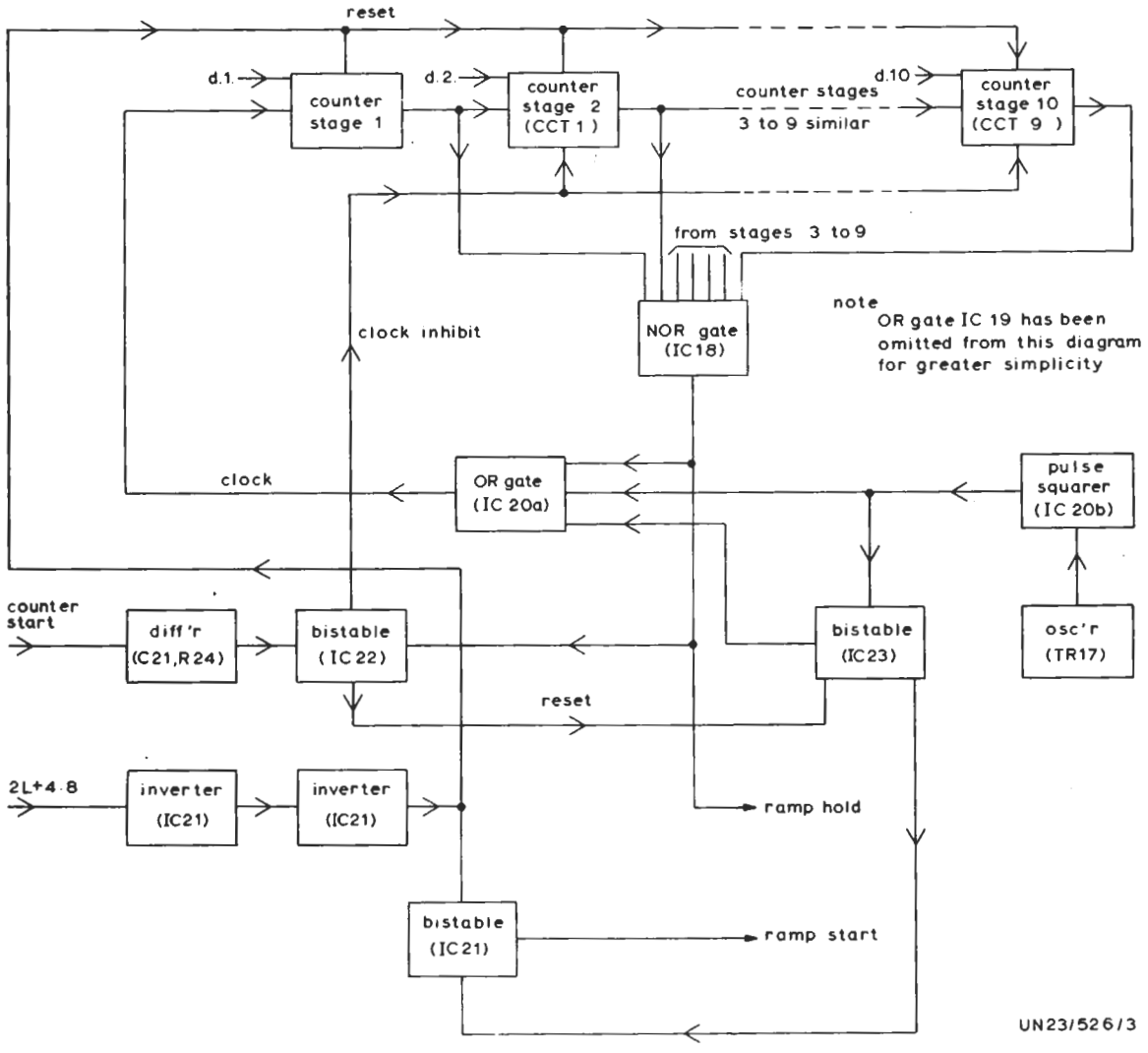

Fig.1 Simplified Block Diagram of the S.i.s. Counter and Logic Unit UN23/526

counter which counts down to zero and in which each stage is clocked by the preceding stage. Twice during each line period (6·4 μs and 38·4 μs after the leading edge of syncs) a 10-bit word is read into the set inputs of the counter, via resistor networks which function as interface stages and change the logic from TTL to MECL. While the reading-in process is taking place, the clock inputs to stages 1IC1 to 9IC1 are inhibited by the output of an RS bistable stage which forms part of IC22 (pins 8 to 13). During the inhibit period input pins 6 and 8 of the counter bistables are held at logic 1.

When the transfer of the 10-bit word to the counter has been completed, a 2L +9·4 counter-start pulse is applied to PLA 4. This pulse is differentiated and the positive-going edge used to trigger a bistable stage that forms part of IC22. The resulting change of state of the IC22 bistable (pin 8 goes to logic 0) removes the inhibition from the clock inputs of the counter stages and also frees bistable stage IC23 (which had previously been held in the $\overline{Q}$ = 1 condition).

Transistor TR17 and its associated components form a free-running 50-MHz crystal oscillator. The output of the oscillator is applied via OR gate IC20b, which functions as a pulse-squarer, to the J input of bistable stage IC23 and to OR gate IC20a also. IC23 changes state on receipt of the first positive-going edge of the 50-MHz waveform, whereupon pin 9 of IC20a is fed with a logic 0 and clock pulses are applied to the first stage of the counter. At the same time the Q output of IC23 (which is now at logic 1) triggers the bistable stage contained in IC21 (pins 8 to 13); pin 8 of IC21 goes to logic 1 and this change of state is applied to the *Ramp Start* output.

Integrated circuits IC18 and IC19 are NOR/OR gates which are fed from the counter outputs. When the six most significant counter stages have reached zero the OR output of IC19 goes to logic 0, when the remaining counter stages have reached zero the NOR output of IC18 goes to logic 1. This change in the output of IC18 has the following effects:

(a) it closes OR gate IC20a and so prevents any further clock pulses reaching the counter;
(b) it changes the state of the bistable stage in IC22 and hence that of IC23 also;
(c) it provides a ramp-hold signal which is used in the associated sample-and-hold unit to hold the ramp voltage at the level attained.

When the count has reached zero the counter remains in a static state until a positive-going 2L +4·8 pulse is applied to PLA 6. The incoming pulse is passed through a resistor network which functions as an interface device and changes the logic levels from TTL to MECL and it is then inverted twice by gates in IC21. The resulting positive-going MECL pulse is applied to all the reset inputs of the counter to ensure that all stages are in the Q = 0 condition before the arrival of the next ten-bit word. Normally, all the counter stages are already in the Q = 0 condition before the arrival of the reset pulse. However, it is possible for the counter to over-run during the count-down process and the resetting operation is a safety precaution to guard against this possibility.

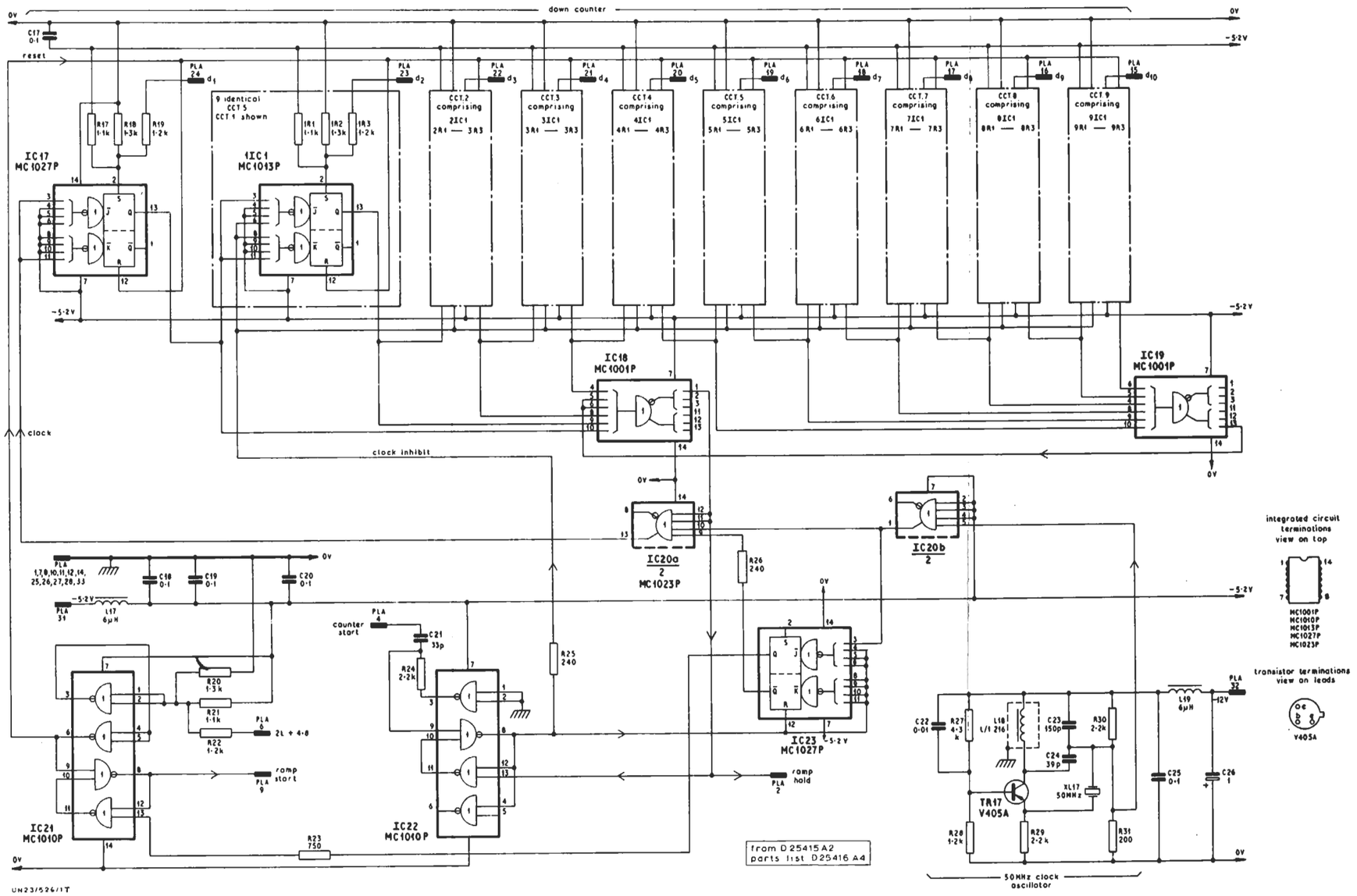

Fig.2 Circuit of the S.i.s. Counter and Logic Unit UN23/526

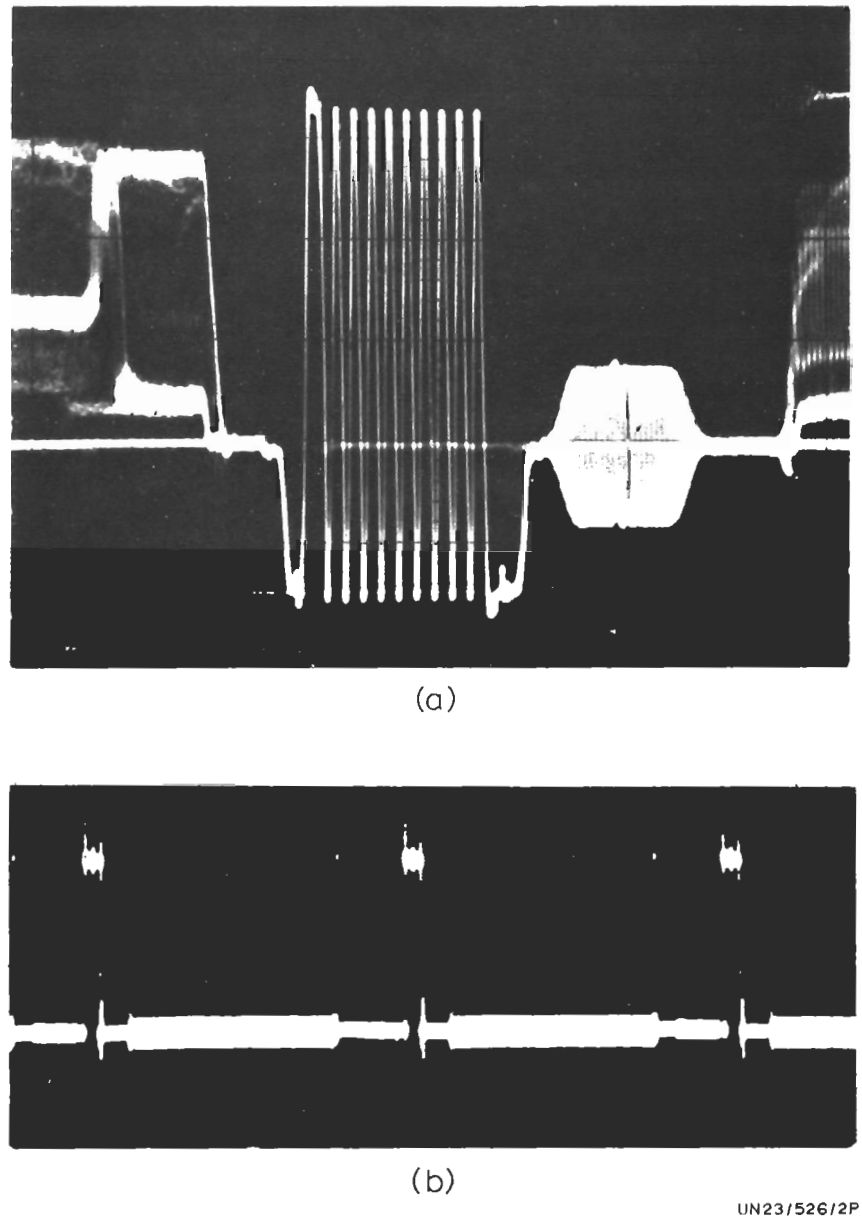

Fig.3 Waveforms in the UN23/526
(a) s.i.s. full count waveform
(b) ramp-hold output about 1V p-p (for a full count)

Maintenance

To check the operation of the unit:

1. Apply a full-count sound-in-syncs signal to the input of the parent decoder. (This signal is shown in Fig.3(a) and can be produced by removing the UN23/528 unit from the associated coder[3].)
2. Check that a *Ramp Hold* waveform, as shown in Fig.3(b), apears at PLA 2. This waveform has two components and consists of: (a) ramphold pulses with a duration of 20 ns occurring at 2L +30μs, (b) pulses with a duration of 1·6μs occurring at 2L +4·8μs.
3. If a *Ramp Hold* output is not produced check that:
   (a) The first counter stage is being fed with gated 50-MHz clock pulses and that successive counter stages are being clocked.
   (b) The Q outputs of the counter stages are set to logic 1 by inputs *d1* to *d10*.
   (c) When the counter has counted down so that all its Q outputs are at logic 0, a logic 1 is produced at the output of gate IC18.

References to Typical Associated Equipment

1. Sound-in-syncs Decoder CD3M/504
2. Sample-and-hold Unit UN23/531
3. Sound-in-syncs Coder CD2M/505

TES 4/71