SOUND-IN-SYNCS SHIFT REGISTER UNIT UN23/527

Introduction

The UN23/527 forms part of the sound-in-syncs coder[1] and is a 21-bit shift register with parallel inputs and serial output[2]. The unit accepts two ten-bit coded words, these are routed to the appropriate positions in the register in such a way that the bits of the words are interleaved. On the receipt of shift pulses, the contents of the register are read out serially, least significant digit first, and a marker pulse is added at the beginning of the digit group. The reading-out process also, by virtue of cross-coupling in the shift register, complements one of the ten-bit inputs; i.e. bits with a value of 1 are changed into bits with a value of 0, and conversely.

The unit is constructed on a printed-wiring card with index pin positions 3, 9 and 15. Connections to the unit are via a 33-way ISEP connector.

General Specification

Inputs

Bit inputs	ten separate inputs, one for each bit of a ten-bit coded word, numbered d1 to d10; derived from UN23/528
Shift inputs	a line-repetitive train of 21 negative-going pulses, pulse duration 50 ns, pulse repetition rate 182 ns; derived from UN23/530
Transfer-odd Input	line-repetitive negative-going pulses; derived from UN23/522
Transfer-even Input	line-repetitive negative-going pulses; derived from UN23/522
Output	a line-repetitive, positive-going pulse train consisting of a marker pulse followed by two ten-bit words interleaved and complemented
Power Requirements	300mA at +5·2V

Circuit Description

A simplified logic diagram of the UN23/527 is given in Fig. 1 and a detailed circuit diagram in Fig. 2.

The shift register consists of 22 JK bistable stages[2] (IC5A to IC17b) and is initially set so that every stage contains a logic 1. Incoming binary-coded samples of the sound signal are applied to the shift register via two-input NAND gates, which open only when a logic 1 is simultaneously present on the appropriate digit and transfer inputs.

To illustrate the operation of the shift register, consider stages IC13b and IC14a; the first (least significant) digit of each sample is applied to the NAND gates which feed these stages. The gate associated with IC13b can open only when a transfer-odd pulse is present and the gate associated with IC14a can open only when a transfer-even pulse is present. Therefore IC13b stores the first digit of odd samples and IC14a stores the first digit of even samples, this sequence is repeated for the other stages of the register and so odd and even samples are effectively interleaved.

Assume that the digit applied to the gate associated with IC13b is a logic 1; the output of the gate becomes a logic 0 and is then inverted again (inside the integrated circuit) so that it becomes a logic 1 at the reset point. At first sight this is the reverse of the required action, for a logic 1 applied to the reset point sets the stage to logic 0 when it should store a logic 1. However, the shift-register stages are cross-coupled so that the application of a shift pulse causes the complement of the bit stored in one stage to be applied to the succeeding stage. This pulse inversion by every stage of the register results in odd-sample bits (which undergo an odd number of inversions in passing through the register) appearing at the output in complementary form and even-sample bits (which undergo an even number of inversions) appearing at the output in their original form.

The stored bits derived from the two samples are read out when a 21-pulse train of shift pulses is applied to the shift input of the unit. Note that, although positive logic is used, the state of the bistables is changed not by the leading edge of the shift pulses but by the trailing edges; this mode of operation is necessary to enable the sampler (described later) to derive a pulse-waveform output from the square-waveform output of the register. Each word is preceeded by a marker bit, which has a value of logic 1 because IC13A stores a logic 1 when in the quiescent state. As the stored bits move through the register under the impetus of the shift pulses the cleared stages of the register are set to logic 1 by the action of IC10b. The J and K inputs of this stage are connected together and returned to a positive potential, therefore the stage changes state each time it receives a shift pulse. Before each shift-pulse sequence, IC10b is primed by the application of a transfer-even pulse to the reset input; therefore the stage starts each sequence with a logic 0 on the Q output and a logic 1 on the $\bar{Q}$ output. The combination of the alternation of IC10b with the cross-coupling between stages results in the entire register being set to logic 1 at the completion of a shift sequence.

During a shift-pulse sequence, the output from IC13A alternates between logic levels 0 and 1 in

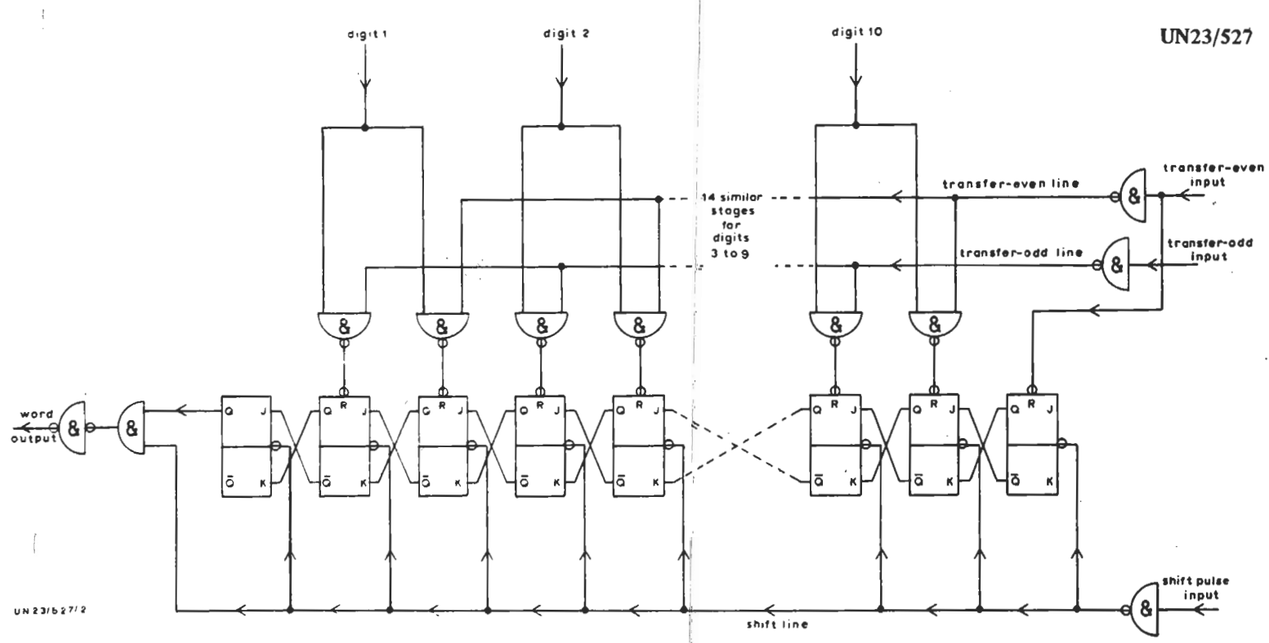

Fig. 1 Simplified Logic Diagram of the UN23/527

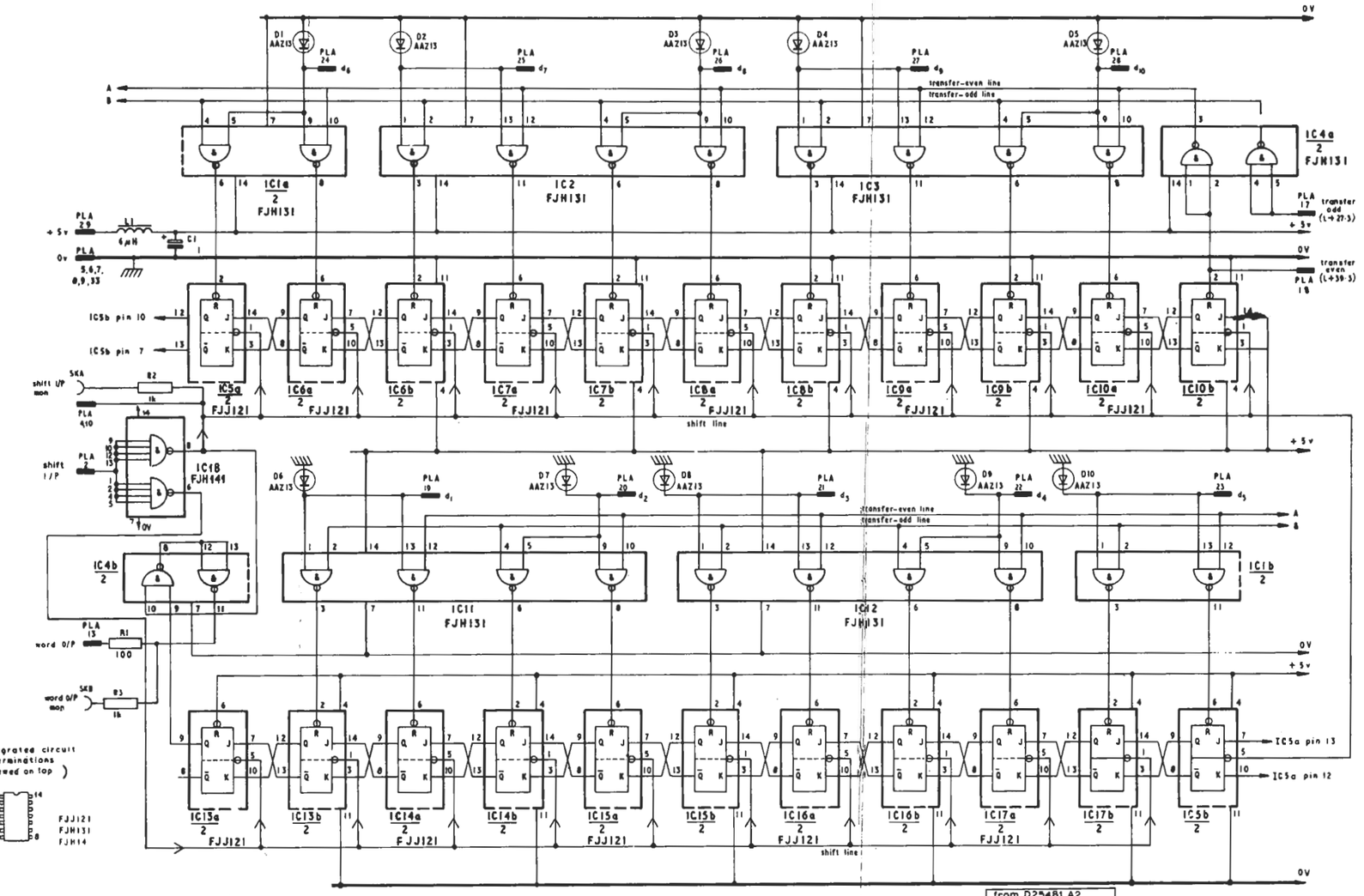

Fig. 2 Circuit of the UN23/527

accordance with the information which is being read out from the register. This waveform is fed to a NAND gate in IC4b where it is sampled by comparison with shift pulses; the input and output waveforms to the sampler for the first six bits of a word are shown in Fig. 3. The resulting pulse waveform is fed, via an inverter which restores it to the correct polarity, to the word output of the unit.

References

1. Sound-in-syncs Coder CD2M/505.
2. Instruction GP1: *Switching Circuits and Logic*

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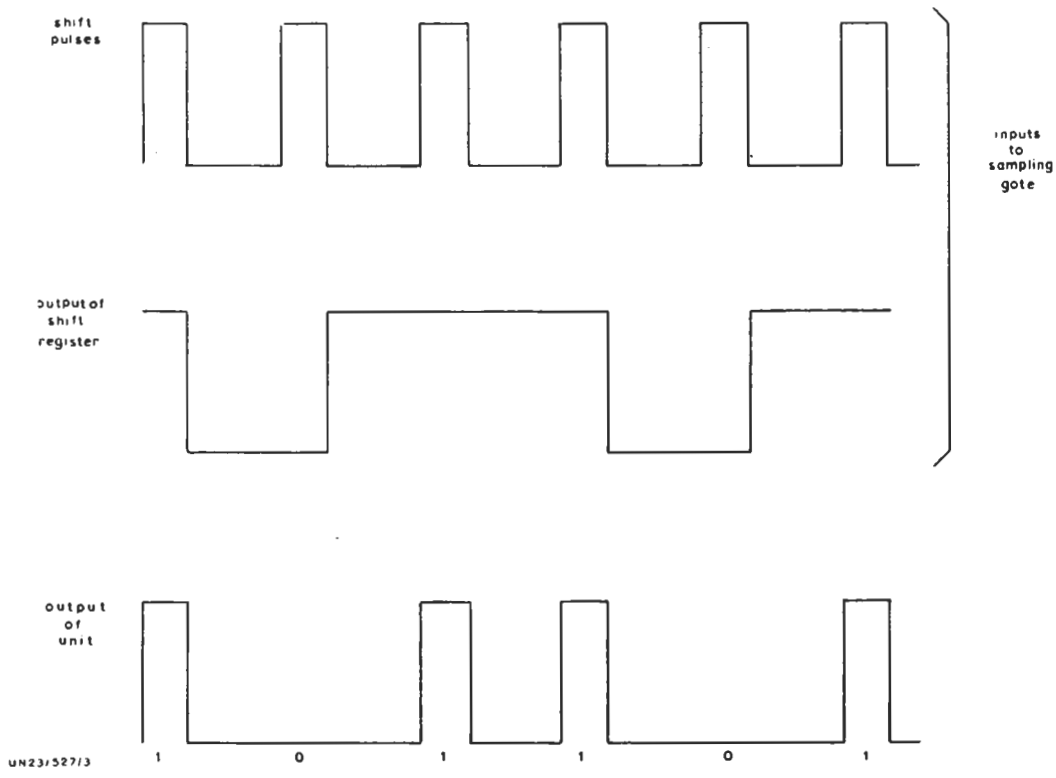

Fig. 3 Input and Output Waveforms of Sampler IC4B