S.I.S. SYNC REGENERATOR UN23/529

Introduction

The UN23/529 forms part of a sound-in-syncs decoder[1]. The unit constructs a standard mixed-sync waveform (i.e. one in which the equalising pulses are restored to normal duration) by examining separated syncs to detect the presence of the first half-line equalising pulse in each field and then gating in the appropriate portions of the following input signals:

line syncs
broad pulses
equalising pulses.

In addition to the mixed-sync output the unit provides the following output waveforms in both positive and negative polarities:

field blanking pulses
field pulses
broad pulses
broad pulse sample pulses.

The UN23/529 is constructed on a printed-wiring card with index-pin numbers 3, 7 and 11. Input and output connections are made via a 33-way ISEP connector; monitor sockets for the mixed-sync and negative-going field-pulse outputs are provided on the front panel of the unit. Power supplies at +5V and −5V are required.

General Specification

Input Signals (All inputs must be at the correct TTL/DTL logic levels.)

Separated Mixed Syncs	positive-going
Line Syncs	positive-going
Equalising Pulses	positive-going
Broad Pulses	negative-going
Clock Pulses	positive-going at twice-line rate, delayed by 27·4 μs w.r.t. leading edge of syncs
Equalising Pulse Interrogate	positive-going, 1 μs duration, delayed by 32·8 μs w.r.t. leading edge of syncs

Output Signals(all at TTL logic levels)

Regenerated Mixed Syncs	conventional polarity
Field Blanking Pulses	both positive-going and negative-going
Field Pulses	both positive-going and negative-going
Broad Pulse Period	both positive-going and negative-going
Broad Pulse Sample	both positive-going and negative-going

Ambient Temperature Range	0°C to 70°C
Power Requirements	210 mA at +5V
DTL and TTL Logic Levels	logic level 1, about +3·5V (+5V max.) logic level 0, about 0V (+0·4V max.)

General Description

A simplified block diagram of the UN23/529 is given in Fig.1. The main function of the unit is to regenerate standard mixed-sync pulses and it does this by a mixture of gating and counting techniques.

Bistable stages IC4a-IC4b and IC4c-IC4d each control the operation of a pair of *Nand* gates; these gates pass line-sync pulses, equalising pulses or broad pulses according to their state and thus determine the composition of the regenerated mixed-sync signal. The sequence of events in the unit is determined (for normal operation) by two counters, a divide-by-625 counter and a divide-by-15 counter. Both counters are clocked at twice-line frequency and are reset to zero at the start of each field (4·8 μs before the first equalising pulse). The divide-by-625 counter initiates the start of each field sequence and the divide-by-15 counter ensures that broad pulses are inserted in the correct position between the two blocks of equalising pulses.

The unit contains also a broad-pulse detector (IC15a) which ensures that broad pulses are routed to the output of the unit at the appropriate time if a non-sync cut upsets the normal sequence of operations.

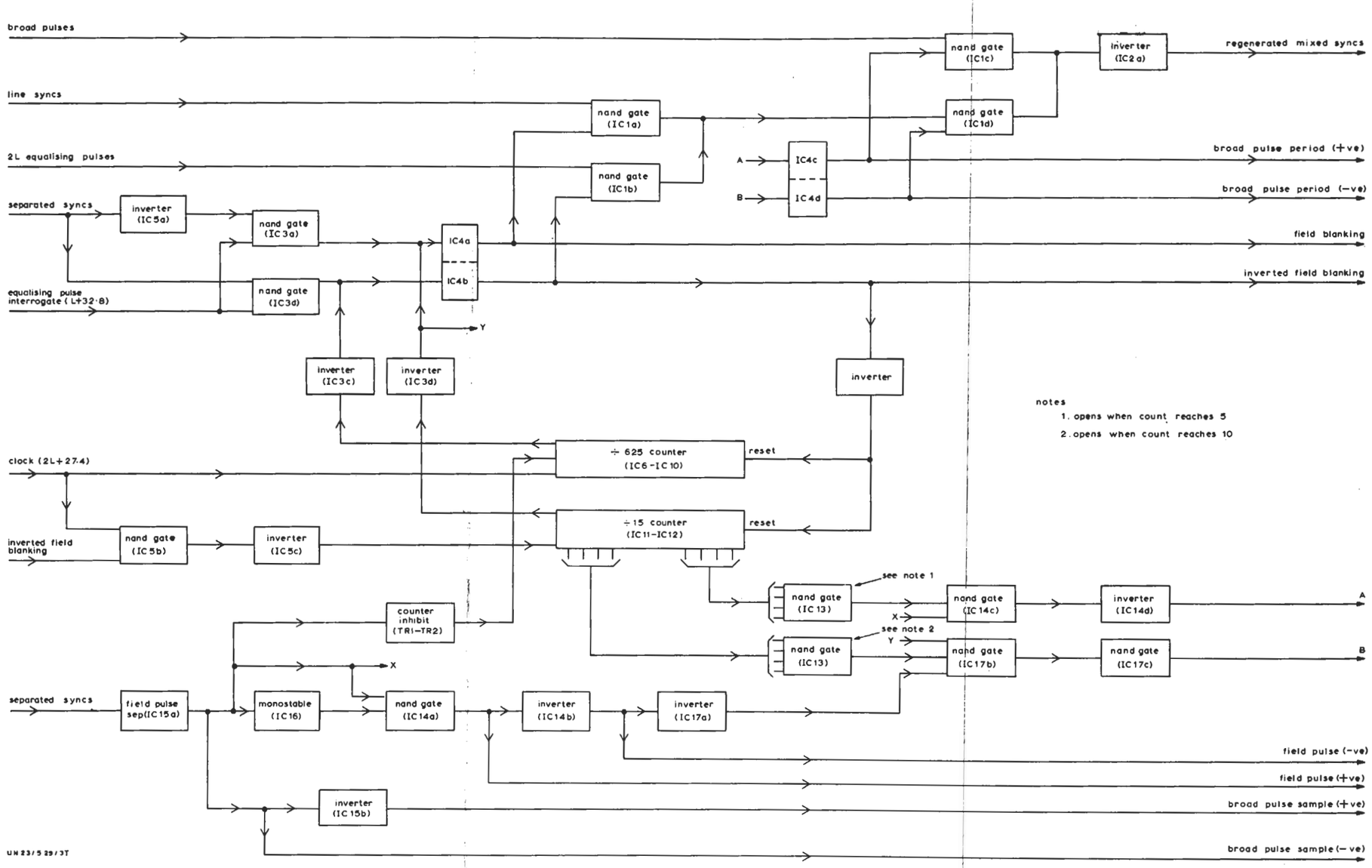


Fig. 1 Simplified Block Diagram of the UN23/529

Circuit Description

A circuit diagram is given in Fig.2 and waveforms present at various points in the unit are shown in Fig.3.

Sync Regeneration and Counter Circuits

Separated syncs, inverted separated syncs and equalising-pulse-interrogate signals are examined in *Nand* gates IC3a and IC3b to detect the presence of the first half-line equalising pulse in each field. When the equalising pulse is detected, the Q (pin 11) output of the bistable stage formed by IC4a-IC4b falls to logic 0 and the $\overline{Q}$ (pin 8) output rises to logic 1. These changes of state are applied to *Nand* gates IC1a and IC1b respectively with the result that equalising pulses pass through IC1b and line syncs are prevented from passing through IC1a.

When the IC4a-IC4b bistable is set to the $\overline{Q}$ = 1 state, the positive-going pulse developed at pin 8 is differentiated, inverted by IC2b and used to reset both counters to zero. The $\overline{Q}$ output is fed also to *Nand* gate IC5b, together with a feed of twice-line frequency (2L + 27·4 μs) clock pulses. When both inputs to the gate are at logic 1, IC5b provides a logic 0 output which is inverted by IC5c and used to start the divide-by-15 counter.

IC13 comprises two four-input *Nand* gates which are fed from various sections of the divide-by-15 counter. When the count reaches 5 the output of one of the gates (pin 1 to pin 6) changes from logic 1 to logic 0. At this time pin 2 of *Nand* gate IC14c is at logic 1, therefore the output of IC14c changes from logic 0 to logic 1 and that of inverter stage IC14d changes from logic 1 to logic 0. This logic 0 is applied to pin 2 of IC4c and triggers the bistable stage formed by IC4c-IC4d into the Q (pin 3) = 1 state. The IC4c-IC4d bistable controls the action of *Nand* gates IC1c and IC1d and it remains in the Q = 1 state from the time that the divide-by-15 count reaches 5 until the count reaches 10. During this period broad pulses pass through IC1c and equalising pulses are prevented from passing through IC1d.

When the divide-by-15 count reaches 10, the output of the second IC13 *Nand* gate (pins 8 to 13) changes to logic 0; as a result the output of IC17b changes to logic 1 and that of IC17c changes to logic 0. Thus the IC4c-IC4d bistable stage is triggered into the Q = 0 state and equalising pulses are once more allowed to pass through gate IC1d.

When the divide-by-fifteen count reaches 15, a logic 1 is applied to inverter stage IC3d and thus a logic 0 is applied to pin 3 of bistable stage IC4a and IC4b. The bistable is triggered into the Q(pin 11) = 1 state; this inhibits the passage of equalising pulses through IC1b and allows line sync pulses to pass through IC1a. For normal operation a count of fifteen is reached 27·4 μs after the leading edge of the first line which does not contain a half-line equalising pulse. This action is confirmed if the sync-examination circuit finds no half-line information present in the separated syncs signal at L + 32·8 μs.

Field Pulse Separator

The field pulse separator ensures that broad pulses are inserted at the correct point in the field waveform in the event of a non-sync cut momentarily upsetting the normal operating sequence.

IC15a is an integrator, with a time constant of approximately 10 μs, which detects the presence of broad pulses. When a broad pulse is detected the output of IC15a changes to logic 0 and, via IC14c and IC14d, triggers the bistable stage IC4c-IC4d into the Q (pin3) = 1 state. Note that for normal operation the bistable is triggered 14·6 μs (10 + 32 − 27·4) earlier when the divide-by-15 count reaches 5.

The output of IC15a also triggers the monostable stage formed by IC16. The duration of the unstable state of IC16 is approximately 2·5 lines and at the end of this period the trailing edge of the output pulse is differentiated and fed, via a chain of *Nand* gates and inverters, to the IC4c-IC4d bistable stage which is then reset to the Q = 0 condition.

Counter Inhibit Circuit

If the video signal fed to the parent decoder consists of line-syncs only, it is necessary to ensure that the output of the UN23/529 unit shall consist of line-syncs only; this is done by inhibiting the operation of the divide-by-625 counter when a signal which contains only line sync pulses is applied to the Separated Sync input of the unit.

Transistors TR1 and TR2 form a counter-inhibit circuit. Under normal conditions separated broad pulses are peak-rectified by TR1 and fed via emitter-follower TR2 to the J and K inputs (See Instruction GP1) of the first stage of the counter (IC6a). Thus, normally, the J and K inputs of IC6a are held at logic level 1. When broad pulses are not present in the separated-sync feed to the unit, the J and K inputs of IC6a fall to logic 0 and the operation of the counter is inhibited.

Additional Outputs

In addition to generating a standard mixed-sync waveform the UN23/529 provides several other output signals. The points in the circuit from which the signals are obtained are listed below.

Broad Pulse Period (+ve)	IC4c, pin 3
Broad Pulse Period (−ve)	IC4d, pin 6
Field Blanking	IC4a, pin 11
Inverted Field Blanking	IC4b, pin 8
Field Pulse (+ve)	IC14a, pin 8
Field Pulse (−ve)	IC14b, pin 11
Broad Pulse Sample (+ve)	IC15b, pin 6
Broad Pulse Sample (−ve)	IC15a, pin 8

Note that not all these outputs are used for existing[1] sound-in-syncs equipment.

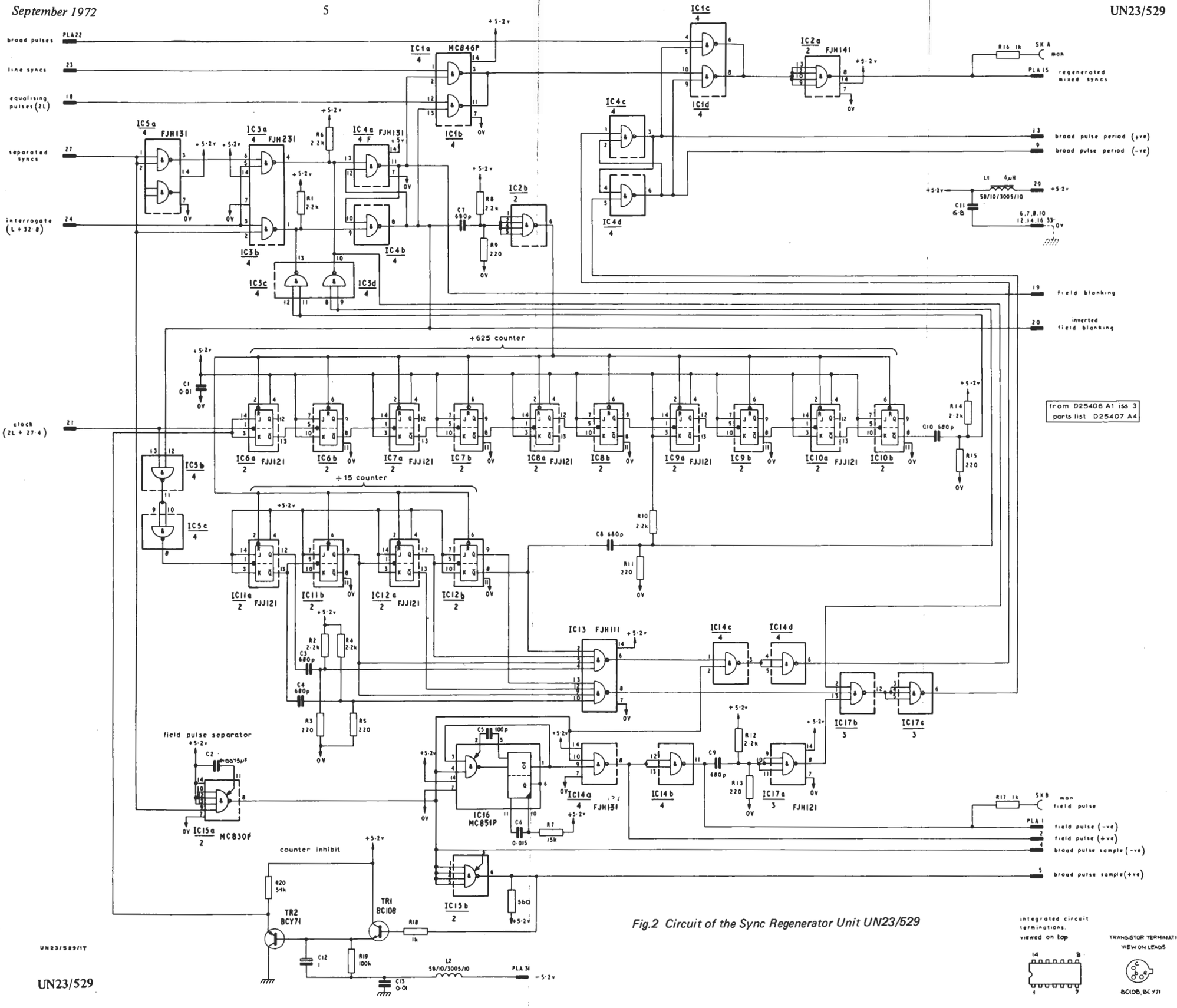


Fig.2 Circuit of the Sync Regenerator Unit UN23/529

Maintenance

Many faults in logic units are of a mechanical nature; therefore a thorough check of the printed-wiring board for dry joints and hairline cracks is recommended as the first step in fault finding.

The waveforms given in Fig.3 show:

input signals, 3(a) and 3(b);

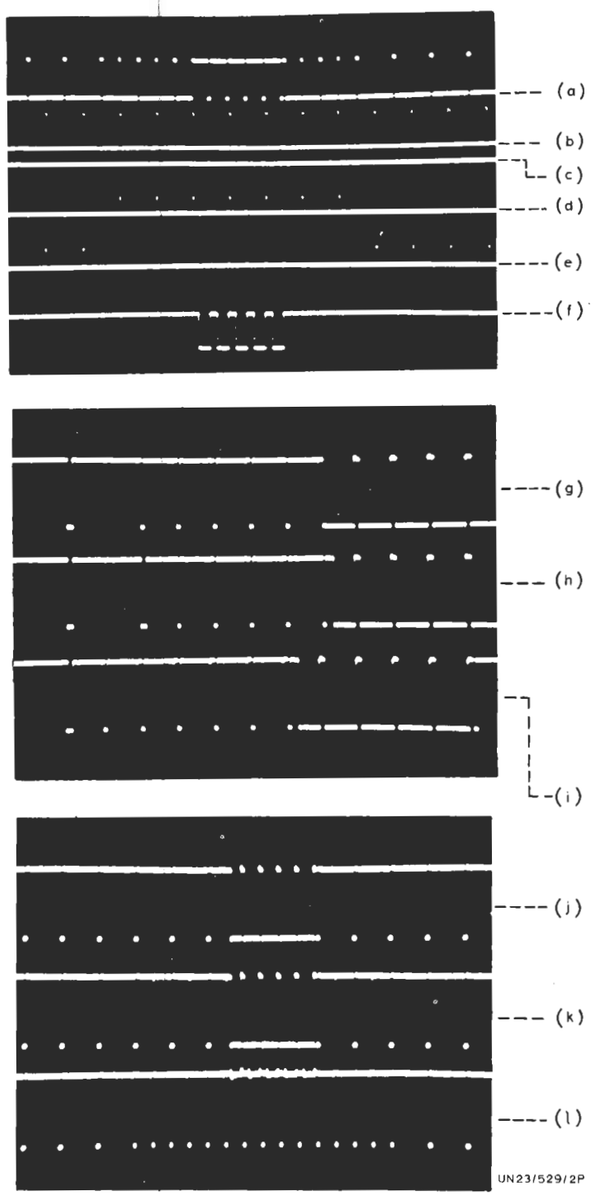
waveforms present at various points in the circuit for correct operation, 3(c) to 3(g);

waveforms of specific fault conditions, 3(h) to 3(l).

References to Typical Associated Equipment

1. Sound-in-syncs Decoder CD3M/504

TES 6/71



Separated Syncs

Equalising Pulse Interrogate

IC3b pin 1

IC3a pin 4

IC2b pin 6 (counter reset)

IC15a pin 8

Correct output on fields where the first equalising pulse occurs in a line-rate position.

Failure of divide-by-625 counter. First equalising pulse replaced by sync pulse and first broad about 10 μs too narrow (i.e. the integration time of IC15a). On alternate fields the first equalising pulse occurs at half-line points and is detected by the interrogate pulse.

Failure of divide-by-5 counter. First broad 10 μs too narrow.

Interrogate pulse (L + 32·8) missing and equalising pulse not inserted.

Failure of bistable IC4a-IC4b; hence no equalising pulses.

Failure of bistable IC4c-IC4d; hence no broad pulses

Fig.3 Waveforms in the UN23/529