SOUND IN SYNCS SAMPLE AND HOLD UNIT UN23/530

Introduction

The UN23/530 forms part of a sound-in-syncs coder[1]. It consists of:

sample and hold circuit
ramp generator
voltage comparator
shift-pulse generator

The unit operates in conjunction with a counter-and-clock unit[2] and a shift register[3].

The audio input to the unit is sampled at twice-line frequency and is then applied, via a storage capacitor, to one input of a voltage comparator. A ramp voltage, which starts when the associated counter-and-clock unit begins to count, is applied to the other comparator input. When the ramp amplitude exceeds that of the sampled audio signal the comparator produces a pulse which stops both ramp and counter. The state of the counter when this occurs is a digital representation of the audio sample.

The shift pulse generator provides pulses for the operation of the associated shift register.

The UN23/530 is constructed on a printed-wiring card fitted with a 33-way ISEP connector and with index-pin numbers 3, 7 and 13. Power supplies at +12V, −12V, +5V and −5V are required.

General Specification

Input Signals

Audio	maximum level +7 dB w.r.t. 1 mW, input impedance 600 ohms
2L Sample	positive-going pulses at twice-line-frequency with a duration of 2·35 μs, obtained from the UN23/522 (TTL logic)
Counter Start (2L + 4·8)	twice-line-frequency pulses, delayed 4·8 μs w.r.t. leading edge of syncs, obtained from the UN23/522 (TTL logic)
Ramp Start	twice-line-frequency pulses, obtained from the UN23/528 (MECL logic)
Ramp Capacitor S/C	twice-line-frequency pulses, obtained from the UN23/528 (MECL logic)
L + 0·1 to L + 3·8	positive-going line-frequency pulses, delayed 0·1 μs w.r.t. leading edge of syncs, obtained from the UN23/522 (MECL logic)

Output Signals

Counter Gate	twice-line-frequency pulses, used in the UN23/528 (MECL logic)
Shift Pulse Output	a line-repetitive train of 22 negative-going pulses, pulse duration 50 ns, pulse repetition rate 182 ns, used in the UN23/527 (TTL logic)

Power Requirements	120 mA at +12V 110 mA at −12V 55 mA at +5V 70 mA at −5V

Logic Levels

TTL	logic level 1, about +3·5V (+5V max.) logic level 0, about 0V (+0·4V max.)
MECL	logic level 1, about −0·75V (−0·7V max.) logic level 0, about −1·75V (−1·5V max.)

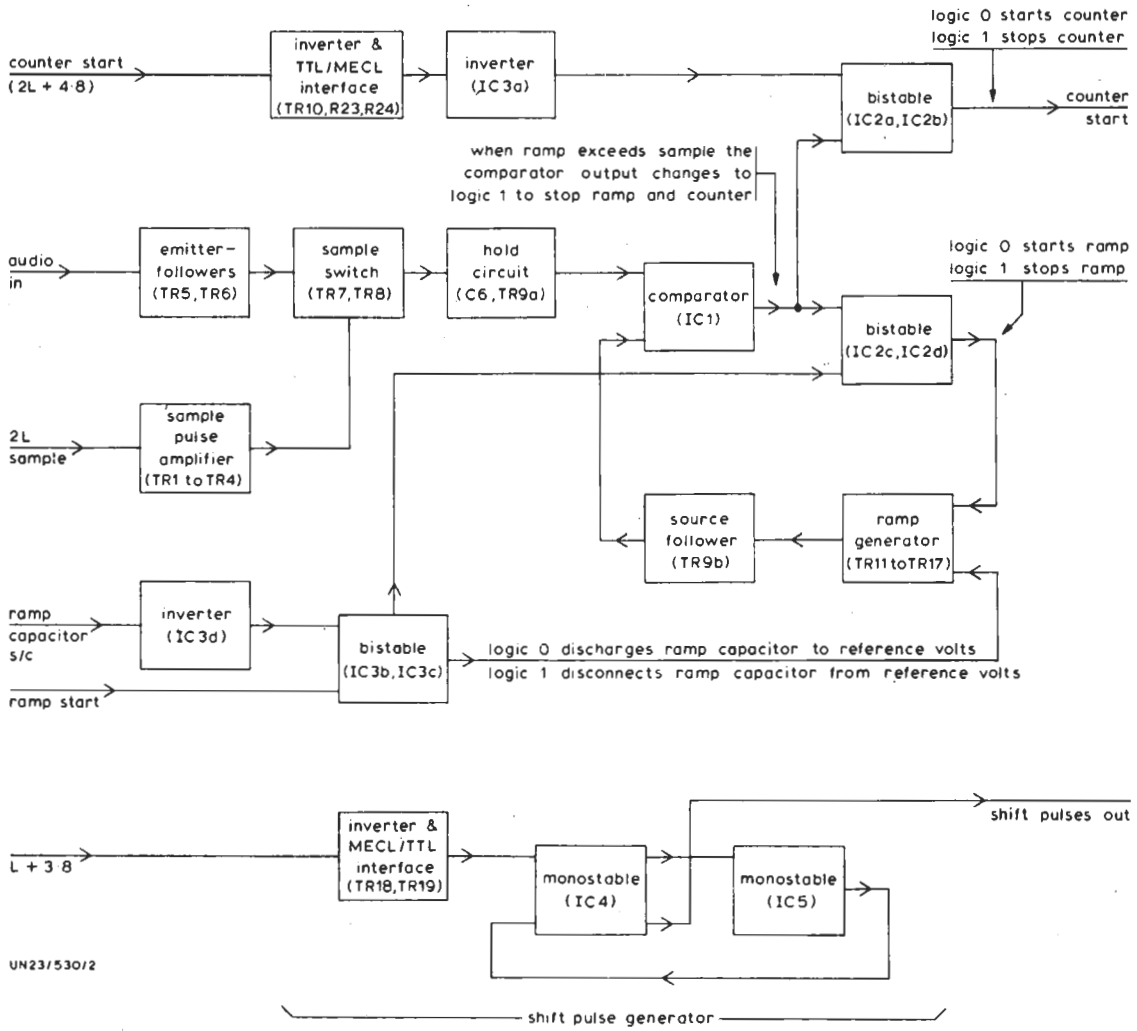


Fig. 1 Block Diagram of the UN23/530

Circuit Description

A block diagram of the UN23/530 is given in Fig. 1, a circuit diagram in Fig. 2 and waveforms at various points in the unit in Fig. 3.

Sample and Hold

The audio input signal is applied, via complementary emitter-followers TR5 and TR6, to a solid-state switch which consists of n-channel and p-channel field-effect transistors (TR7 and TR8) connected in parallel. The switch is driven by anti-phase twice-line-frequency pulses which are derived from the *2L Sample* input by the long-tailed pairs TR1, TR4 and TR2, TR3. The use of anti-phase sample pulses reduces the effect of switching transients on the output.

Each time the sample switch conducts, a sample of the audio signal is stored on C6. From C6 the sample is fed, via source-follower TR9a which provides the high input impedance needed to maintain the charge on C6, to comparator stage IC1.

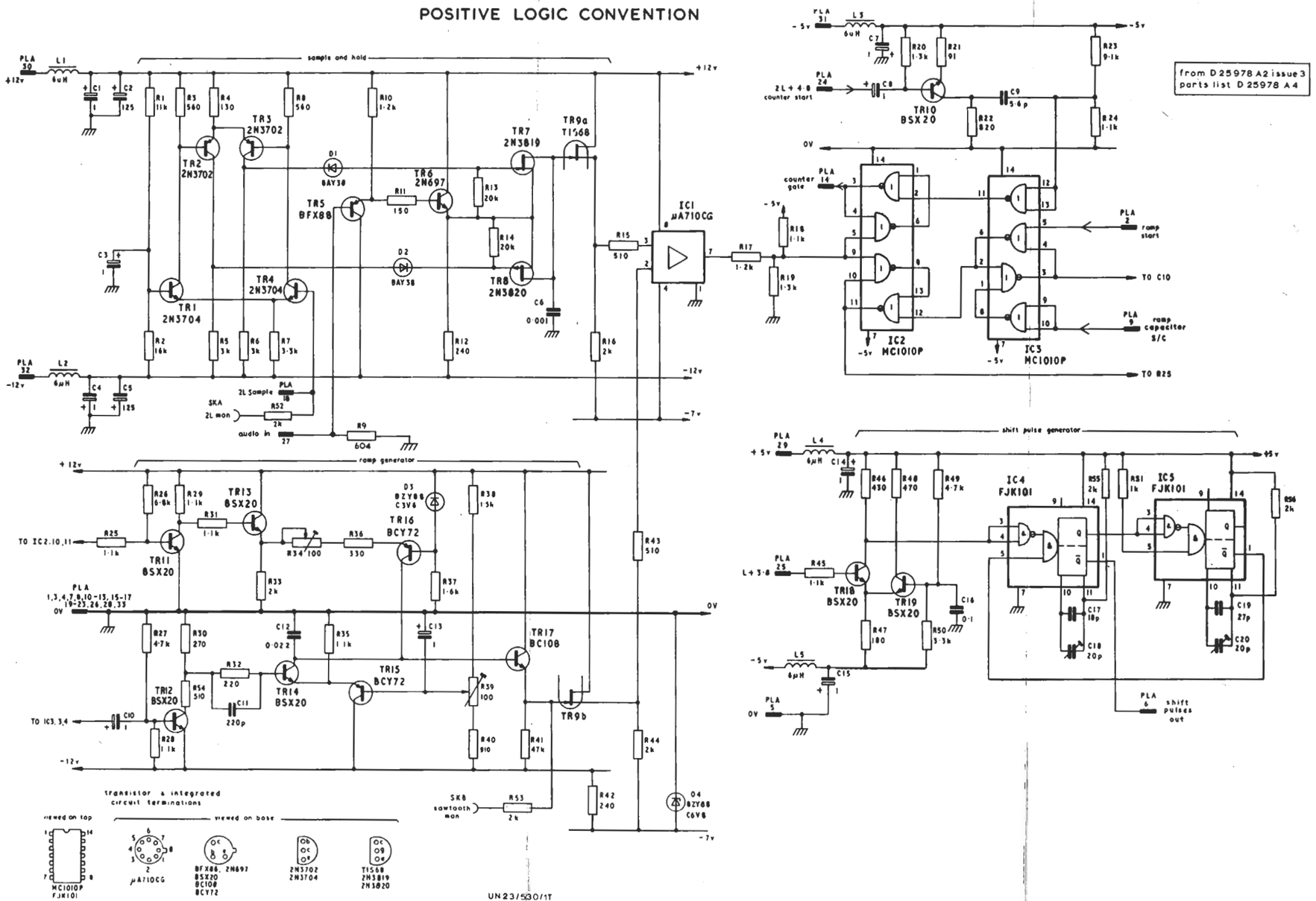
Ramp Generator

The ramp generator consists, basically, of a capacitor (C12) which can either be charged from a constant-current source (TR16) or discharged to a reference voltage (TR15 emitter). The operation of the circuit is described below.

An incoming negative-going *Ramp Capacitor S/C* pulse is inverted by IC3d. The resulting logic 1 pulse changes the state of the bistable stage formed by IC3b and IC3c, and causes a logic 0 to appear at pin 3 of IC3c. This pulse is fed, via C10, to TR12 which cuts off. The rise in the collector potential of TR12 drives TR14 into conduction and so connects the ramp capacitor (C12) to the reference potential present at the emitter of TR15. The reference potential is determined by the setting of R39 and has a nominal value of −2·5 volts.

Twice in each line period a *Counter Start* pulse at TTL logic level 1 is inverted by TR10 and differentiated by C9, R23 and R24. The resistors R23 and R24 act also as a TTL/MECL interface network and ensure that the differentiated spike caused by the leading edge of the pulse is at MECL logic level 0. The spike is inverted by IC3a and the resulting positive-going pulse changes the state of the bistable stage formed by gates IC2a and IC2b, and so causes a logic 0 to appear at the *Counter Gate* output, PLA 14. This pulse is fed to the associated

POSITIVE LOGIC CONVENTION



UN23/530/1T

from D25978 A2 issue 3 parts list D 25978 A4

Fig. 2 Circuit of the UN23/530

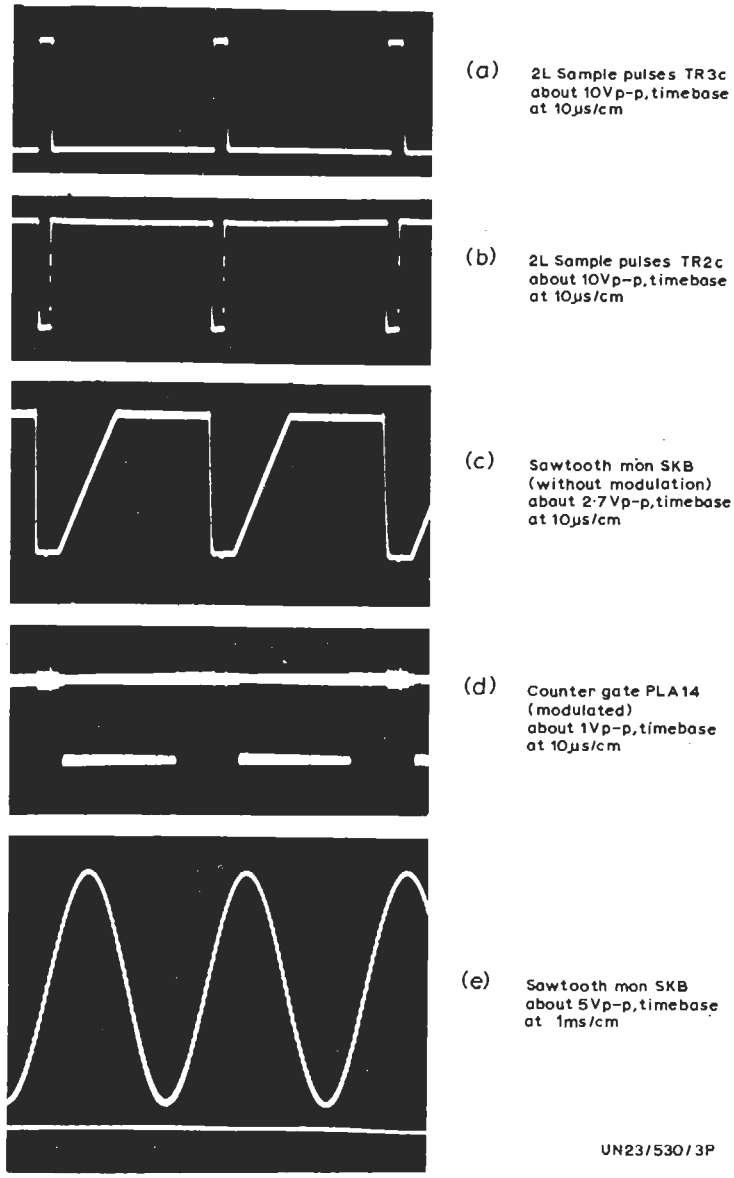


Fig. 3 Waveforms

counter-and-clock unit to initiate the start of the count.

On receipt of a *Ramp Start* signal the bistable stage formed by gates IC3b and IC3c changes state with the result that TR12 conducts, TR14 is cut off, and the ramp capacitor is disconnected from the reference potential.

The *Ramp Start* pulse is used also (via IC3c) to change the state of the bistable formed by IC2c and IC2d; when the stage changes state, pin 11 of IC2d goes to logic 0 and transistor TR11 is cut off. When TR11 cuts off TR13 conducts and TR16, which functions as a constant-current generator for the ramp capacitor, conducts also. The ramp capacitor C12 charges in a linear fashion and the resulting ramp voltage is fed, via emitter follower TR17 and source-follower TR9b, to pin 2 of comparator stage IC1.

Voltage Comparator

Voltage comparator IC1 accepts both the sample-and-hold (pin 3) and the ramp generator (pin 2) outputs. When the ramp amplitude exceeds that of the audio sample, the output of the comparator changes from logic 0 to logic 1 (TTL levels). This change in level is fed via a TTL to MECL interface network (R17, R18, R19) to the two bistable stages contained in integrated circuit IC2 and causes both stages to change state; pin 11 of IC2d goes to logic 1 and turns off the constant-current generator, pin 3 of IC2a goes to logic 1 and stops the count in the associated counter-and-clock unit.

Shift Pulse Generator

The shift-pulse generator ocontains two monostable multivibrators, IC4 and IC5, which can be triggered either by positive-going edges (on pin 5) or by

negative-going edges (on pins 3 and 4).

The incoming positive-going L+3·8 pulse (MECL logic) is inverted and changed to TTL logic by the long-tailed pair comprising transistors TR18 and TR19. From the collector of TR18 the resulting logic 0 pulse is applied to pins 3 and 4 of IC4 which is triggered into its unstable (Q = 1) state. The Q output of IC4 remains in the logic 1 state for a time (about 50 ns) which is determined by the time-constant components C17, C18 and R55. When IC4 returns to its stable state it triggers monostable stage IC5 the $\overline{Q}$ output of which goes from logic 1 to logic 0. IC5 remains in the $\overline{Q}$ = 0 state for a period determined by C19, C20 and R56 and then returns to the stable ($\overline{Q}$ = 1) state. This change of state re-triggers monostable stage IC4 and perpetuates the sequence, which continues until the end of the L + 3·8 pulse.

The Shift Pulses output is taken from the $\overline{Q}$ output of IC4 and consists of a train of 21 negative-going pulses, recurring at line rate, for use in an associated shift-register unit. The pulse repetition rate is determined by IC5 and is about 182 nano-seconds.

Maintenance Adjustments

Shift Pulse Generator

The shift pulse generator section of the UN23/530 may need adjustment if components are changed. Adjustment should be undertaken only if a high-grade oscilloscope and a frequency counter are available.

To adjust, proceed as follows:

1. Calibrate the oscilloscope to measure 50 ns accurately, by displaying the 50-MHz output available at *Test Point A* on the associated UN23/528 unit and adjusting the time-base controls accordingly.
2. Use a high-impedance probe to monitor PLA 6 on the UN23/530. Select the second negative-going pulse of the wave train and adjust C18 to make the half-amplitude duration exactly 50 ns.
3. Adjust C20 to set the pulse-repetition rate to approximately 182 ns.
4. Temporarily connect PLA 25 on the UN23/530 to 0V and check that the wave train at PLA 6 is now continuous.
5. Replace the oscilloscope with the frequency counter and set the frequency counter to measure frequency with the time base set to 10 ms.
6. Adjust C20 for a frequency of 5·5 MHz (±2 kHz).
7. Remove the connection between the 0V line and PLA 25.
8. Replace the frequency counter with the oscilloscope and check that a train of 21 negative-going pulses, recurring at line rate, is present at PLA 6.

Ramp Generator

To maintain optimum operating conditions, the pre-set controls on the ramp generator should be adjusted if the unit is changed. Because the adjustment of these controls affects other units, the procedure is given in the Instruction on the parent coder.

References to Typical Associated Equipment

1. Sound-in-syncs Coder CD2M/505
2. Counter and Clock Unit UN23/528
3. Shift Register UN23/527

TES 9/71