SAMPLE AND HOLD UNIT UN23/531

Introduction

The UN23/531 forms part of a sound-in-syncs decoder[1]. It consists of: a ramp generator, a sample-and-hold circuit, a muting circuit and a shift-pulse generator.

The operation of the ramp generator is synchronised to that of an associated Counter and Clock Unit[2]; the generator starts when the counter commences its count down and stops when the counter reaches zero. The ramp voltage is then sampled and held, following which the ramp generator is discharged to await the next counting sequence. The audio output from the sample-and-hold circuit is the analogue representation of the digital signal presented to the Counter and Clock Unit.

The muting circuit mutes the audio output of the unit if an incorrect signal is received by the decoder. A mute is applied rapidly if a fault occurs but it is not removed until the decoded signal crosses a zero voltage point. This precaution reduces the audible effect of the mute on the audio signal.

The shift pulse generator provides pulses for the operation of an associated Shift Register Unit[3].

The UN23/531 is constructed on a printed-wiring card fitted with a 33-way ISEP connector and with index-pin positions 3, 7 and 19. Power supplies at +12 volts, −12 volts, +5 volts and −5 volts are required.

General Specification

Input Signals

Ramp Hold	negative-going pulse at twice line frequency, obtained from the UN23/526 (MECL logic)
Ramp Start/Stop	negative-going pulse at twice line frequency, obtained from the UN23/526 (MECL logic)
Current Start	twice line frequency positive-going pulses delayed by 5·6μs w.r.t. leading edge of syncs (2L +5·6) obtained from the UN23/523 (TTL logic).
Shift Start	negative-going pulse at line frequency, obtained from the UN23/524 (TTL logic)
Shift Stop	positive-going pulse at line frequency, obtained from the UN23/524 (TTL logi)
Line Blanking	negative-going pulse, obtained from the UN23/523 (TTL logic)
Mute	logic 1 for normal conditions, logic 0 when a mute is present, obtained from the UN23/527 (TTL logic)
2L	positive-going pulse at twice line frequency, obtained from the UN23/522 (TTL logic)

Output Signals

Audio	unfiltered sampled audio at a maximum level of +7 dB with respect to 1 milliwatt (when unterminated)
Shift Pulses	line-repetitive train of 22 negative-going pulses, pulse repetition period 182 ns, nominal pulse duration 50 ns. (TTL logic)
Expander Mute	logic 0 for normal conditions, logic 1 when a mute is present (TTL logic)

Power Requirements	110 mA at +12V, 120 mA at −12V 65 mA at +5V, 30 mA at −5V.

Logic Levels

TTL	logic level 1, about +3·5V (+5V max.) logic level 0, about 0V (+0·4V max.)
MECL	logic level 1, about −0·75V (−0·7V max.) logic level 0, about −1·75V (−1·5V max.)

Circuit Description

A block diagram of the UN23/521 is given in Fig.1, a circuit diagram in Fig.2 and waveforms at various points in the circuit in Fig.3.

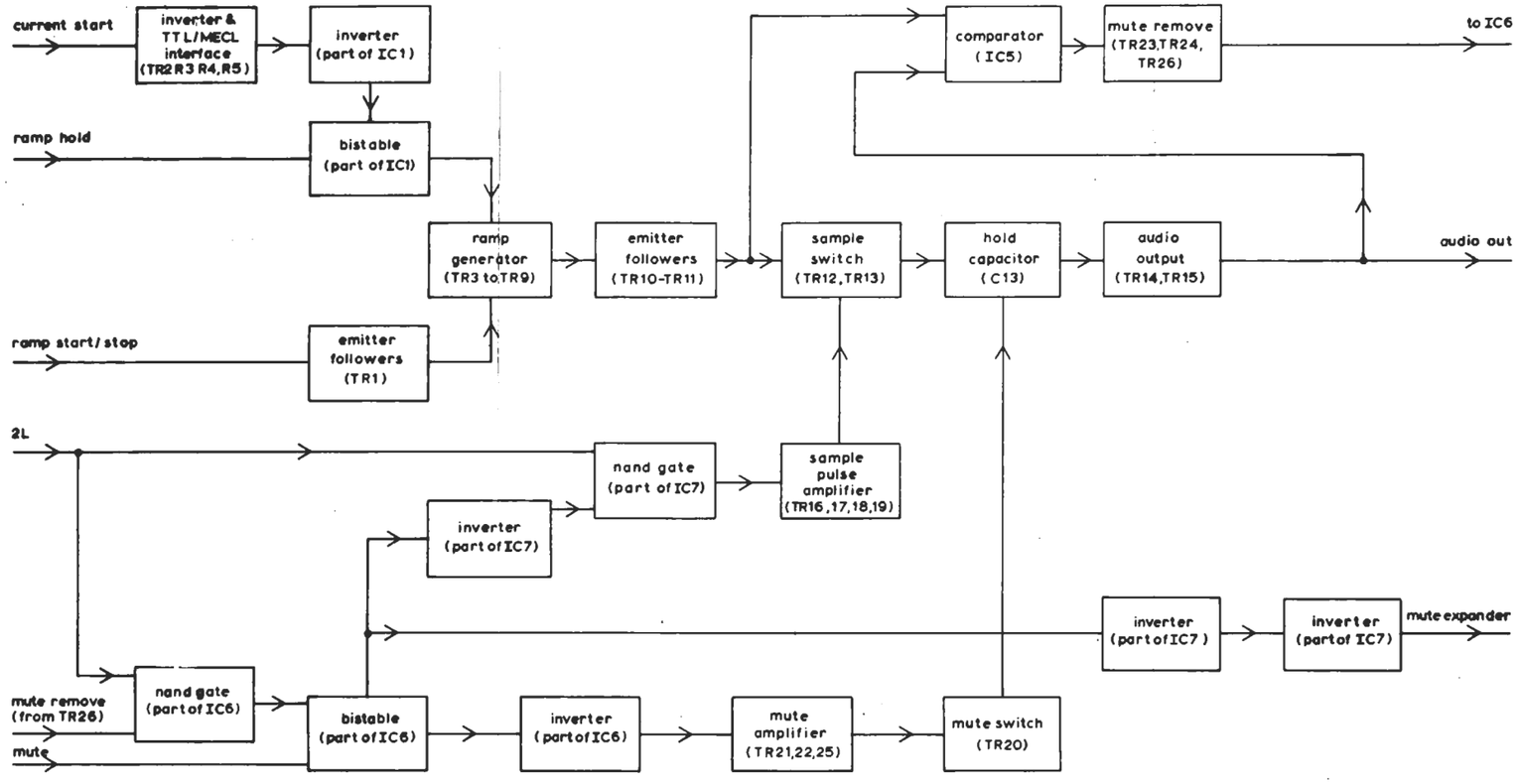

Fig. 1 Block Diagram of the Sample and Hold Unit UN23/531

Ramp Generator

The ramp generator consists, basically, of a capacitor (C11) which can either be charged from a constant-current source (TR7) or discharged to a reference voltage (TR8 emitter). The operation of the circuit is described below.

Before the start of each sample period (at times 2L +4·8μs) a negative-going pulse is applied to the *Ramp Start/Stop* input and passed via emitter-follower TR1 to amplifier-inverter stage TR4. The positive-going pulse developed at the collector of TR4 drives TR6 into conduction and so connects the ramp capacitor (C11) to the reference potential present at the emitter of TR8. The reference potential is determined by the setting of R22 and has a nominal value of −2·5 volts.

At times 2L +5·6μs a *Current Start* pulse at TTL logic level 1 is fed via inverter stage TR2 to a TTL to MECL interface formed by R3, R4 and R5. The resulting MECL logic 0 pulse is inverted by gate 8,9,10 of IC1 and applied to the bistable stage formed by gates 1,2,3 and 4,5,6 of IC1. The output (pin 6) of the bistable stage changes to logic 0 and transistor TR3 cuts off. When TR3 cuts off TR5 conducts and TR7, which functions as a constant-current generator for ramp capacitor C11, conducts also. However, C11 remains, momentarily, in the discharged state because TR6 is still conducting.

At times 2L +9·4μs the *Ramp Start/Stop* signal changes to logic level 1 and TR6 is cut off. Simultaneously C11 starts to charge and the counter in the associated Counter and Clock Unit starts to count down towards zero. When the count reaches zero the *Ramp Hold* input changes to logic level 1, consequently the IC1 bistable stage changes state and cuts off the current generator. The potential across C11 at this time is the analogue representation of the digital signal which has just been counted.

Sample and Hold

The ramp voltage present on C11 is passed via emitter-followers TR9, TR10 and TR11 to the sample-and-hold circuit. TR9 provides a high-impedance load for C11; TR10 and TR11 drive the sample switch formed by field-effect transistors TR12 and TR13. The switch transistors are driven by anti-phase twice-line-frequency pulses derived from the sample pulse amplifier. The use of anti-phase sample pulses reduces the amplitude of switching transients occurring at the output.

Each time the sample switch conducts, the sampled ramp voltage is stored on C13. From C13 the sample is capacitor-coupled to source-follower TR14 and is then fed via emitter follower TR15 to the audio output of the unit.

Sample Pulse Amplifier

Gate 1,2,3 of IC7 inverts the positive-going 2L pulses and feeds the resulting negative-going pulses to the base of TR19. Transistors TR16 to TR19 form a complementary long-tailed pair stage which produces anti-phase sample pulses for use in the sample switch. Under fault conditions (see Mute Circuit) the 2L pulse feed from IC7 to TR19 is inhibited by the action of IC6 and sample pulses are not produced.

Mute Circuit

If the sound-in-syncs signal applied to the decoder is faulty, a logic 0 pulse is developed in an associated Error Detection Unit[4] and fed to the *Mute* input of the UN23/531. The mute pulse changes the state of the bistable formed by gates 8,9,10 and 4,5,6 of IC6 and the bistable output (pin 8) changes to logic 1. The logic 1 pulse is inverted by gate 11,12,13 of IC6 and a logic 0 is fed to TR25. As a result transistors TR25, TR22 and TR21 are cut off and field-effect transistor TR20 is driven into conduction. When TR20 conducts the base of TR14 is effectively earthed, whereupon capacitor C13 is discharged and the audio output of the unit is muted.

Note that the *Mute* input also affects the operation of the gates contained in IC7; when a mute is present the 2L pulses which normally feed TR19 in the sample-pulse amplifier are inhibited, additionally a logic 1 pulse is generated and fed to the *Expander Mute* output of the unit.

Muting is applied rapidly but, after the fault condition which caused the mute has disappeared and the *Mute* input has returned to logic 1, it is not removed until the decoded signal crosses a point of zero potential; this precaution minimises audible thumps on the decoded output. The correct moment for de-muting is determined by differential amplifier IC5 which amplifies any difference between the ramp voltage present at the emitter of TR11 and the reference potential (0V) present at pin 3 of IC5. The gain of the stage, about 14, is given by the ratio of R45 to R44.

Transistors TR23, TR24 and TR26 form a

zero-voltage crossing detector. When the output of IC5 is coincident with the zero-volt reference potential the base of TR23 is also at zero volts; hence both TR23 and TR24 are cut off and the detector output is at +5 volts (i.e. logic level 1). When the voltage at TR23 base exceeds the base-to-emitter potential of TR23 the transistor conducts and the detector output falls to zero volts (i.e. logic level 0). When the voltage at TR23 base exceeds the base-to-emitter potential of TR24, both TR24 and TR26 conduct and the detector output gives a logic 0 output. Thus only on zero-voltage crossing points does the detector give a logic 1 output.

The output of the zero-voltage detector is fed to gate 1,2,3 in IC6 together with a feed of the *2L* input. When a zero-crossing point is detected, provided that it occurs during a 2L sample period, the output of gate 1,2,3 goes negative and changes the state of the bistable stage formed by gates 4,5,6 and 8,9,10. As a result transistor TR20 is cut off and the mute is removed from the audio output. At the same time:

(a) gate 1,2,3 in IC7 is opened and *2L* pulses are fed to TR19 in the sample pulse amplifier;
(b) the *Expander Mute* output changes to logic 0 to indicate that the mute has been removed.

Shift Pulse Generator

The shift pulse generator produces pulses for the operation of an associated Shift Register Unit. The generator consists of two monostable multivibrators, IC3 and IC4, which can be triggered either by positive-going edges (on pin 5) or by negative-going edges (on pins 3 and 4). The generator is controlled by a bistable stage formed by gates 3,4,5,6 and 8,9,10,11 of IC2. The output of the bistable stage (pin 8) changes to the logic 1 state when a negative-going *Shift Start* pulse is applied to pin 11 and the positive-going edge of the transition drives IC3 into its unstable (Q = 1) state for a period determined by the time constant of C13 and R67. When IC3 returns to its stable state the change triggers IC4 into its unstable state for a period determined by the time-constant of C20, C21 and R68. When IC4 returns to the stable state it re-triggers IC3 and the process is repeated until a negative-going *Shift Stop* pulse (derived from the Shift Register Unit when all the sound pulse digits have been read into the register) changes the state of the IC2 bistable stage.

The *Shift Pulse Output* is taken from IC3 and consists of a train of 22 negative-going pulses, with a duration of 50 nano-seconds, recurring at line rate. The pulse repetition rate is determined by IC4 and is nominally 182 nano-seconds.

To ensure that the shift pulse generator operates correctly when the equipment is first switched on, the IC2 bistable stage is initially reset by a pulse derived from the leading edge of line-blanking. This ensures that the *Shift Start* input always causes a transition from logic 0 to logic 1 to occur at the input to monostable stage IC3.

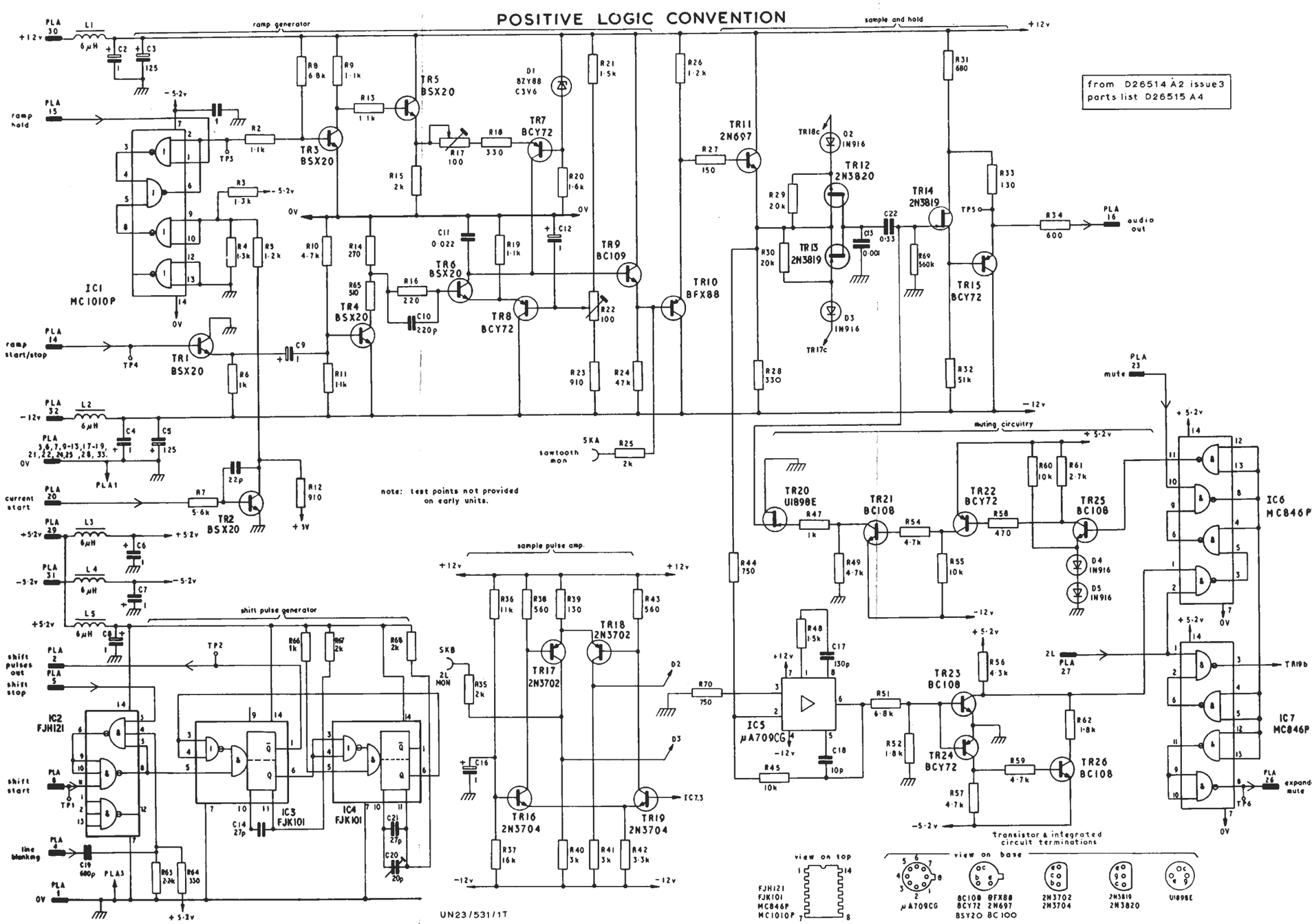

Fig.2 Circuit of the Sample and Hold Unit UN23/531

Maintenance Adjustments

Ramp Generator

To maintain optimum operating conditions, the pre-set controls on the ramp generator should be adjusted if the unit is changed. The parent decoder will, however, continue to operate if these adjustments are not carried out. To carry out the adjustments, feed the decoder from a correctly aligned coder which does not have a signal applied to the audio input.

(i) Ramp Amplitude

Remove the associated AM1/38 unit and, using an extender board and a Painton 15-way plug, feed the signal developed between pins 14 and 15 of the back connector to the high-impedance input of an accurately calibrated ATM/1 or equivalent. Place the UN23/531 unit on an extender board and adjust R17 to obtain a reading on the ATM/1 of −14·5 dB with respect to one milliwatt.

(ii) Ramp Sit

With the UN23/531 still on the extender, monitor SKA (*Sawtooth Mon.*) with an oscilloscope probe. Check that a twice-line-frequency sawtooth is present and that it is modulated by pilot tone. Adjust R22 until the most negative portion of this waveform is at −2·5 volts.

Shift Pulse Generator

The shift pulse generator may need adjustment if components are changed. Adjustment should be undertaken only if a high-grade oscilloscope and a frequency counter are available. To adjust proceed as follows:

1. Feed the decoder with a coded sound-in-syncs signal and place the UN23/531 unit on an extender board. Monitor PLA 2.
2. Remove the UN23/524 unit from the decoder assembly and temporarily strap pins PLA 8 and PLA 10 on the UN23/531.
3. Monitor PLA 2 on the UN23/531 unit with a high-impedance probe. The display obtained should consist of a continuous train of negative-going pulses of repetition period 182 nano-seconds.
4. Replace the oscilloscope with the frequency counter. Set the frequency counter time base to 10 milli-seconds and adjust C20 for a frequency of 5·5 MHz ±2 kHz.
5. Remove the strap between PLA 8 and PLA 10. Replace the UN23/524 unit. Monitor PLA 2 on the UN23/531 unit with the oscilloscope probe and confirm groups of 22 pulses recur at line rate.
6. Remove the extender board and replace the UN23/531 unit.

References to Typical Associated Equipment

1. Sound-in-syncs Decoder CD3M/504
2. Sound-in-syncs Counter and Clock Unit UN23/526
3. Sound-in-syncs Shift Register UN23/524
4. Sound-in-syncs Error Detection Unit UN20/527

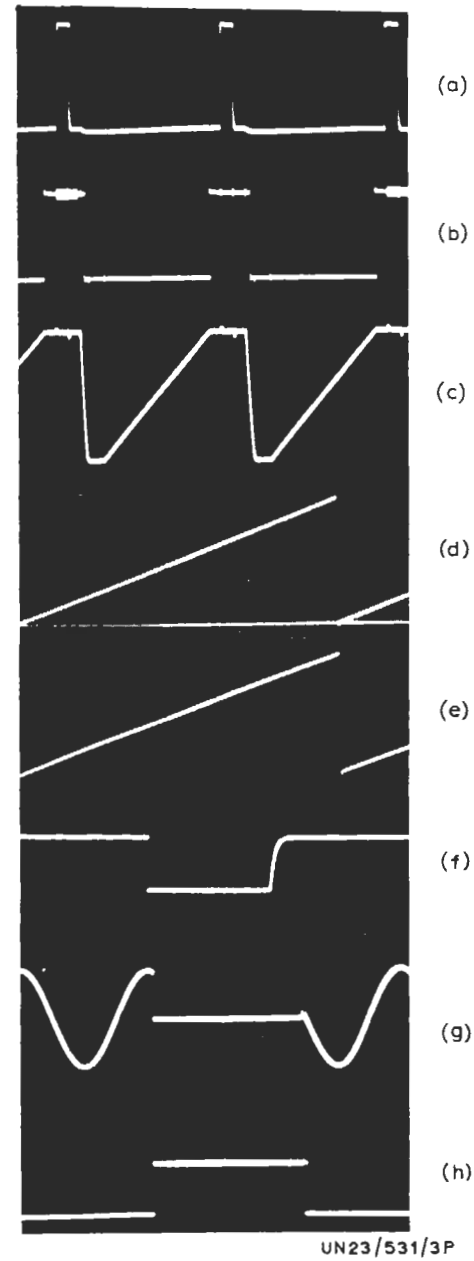

Fig.3 Waveforms in the UN23/531

(a) SKB 2L sample pulses about 20V
(b) current start/stop about 4V (on full count)
(c) sawtooth mon SKA about 5V (on full count)
(d) sawtooth mon SKA, field rate (check counter)
(e) audio output TR15e about 5V
(f) mute signal about 5V (check mute)
(g) muted audio TR15e 4V (check mute)
(h) expander mute output 5V (check mute)
Waveforms f,g,h time-base at 2ms/cm, all waveform amplitudes are p-p.
For waveform (d) set the links in the UN23/528 unit (in the coder) to CHECK.
For waveforms (f), (g), (h) set link LK1 in the UN20/527 unit to CHECK.

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