EXECUTIVE LOGIC UNIT UN23/533

Introduction

The UN23/533 accepts four d.c. input signals and uses these, after suitable decoding, to operate relays and indication lamps. Provision is made also for three reset signals to be applied.

The unit is designed for use with a Television Automatic Monitor MN2M/518. It is built on a printed wiring board which is mounted on a CH1/43A chassis with index pegs in positions 1, 3 and 15.

General Specification

Logic levels	
Logic 1	2·6 volts minimum
Logic 0	0·4 volt maximum
Power Requirements	+12 volts at 80 mA
	+6 volts at 120 mA
	+5 volts at 40 mA
Pin connections	25-way ISEP plug

TABLE 1

Line	Logic Input				Resultant Action				
	PLA2	PLA3	PLA4	PLA5	Tx C/O	Main Feed	Res. Feed	RLA	RLB
1	1	0	0	0	off	on	off	energised	de-energised
2	1	0	0	1	off	off	on	energised	energised
3	1	0	1	0	off	on	off	energised	de-energised
4	1	0	1	1	on	on	off	de-energised	de-energised
5	1	1	0	0	on	off	on	de-energised	energised
6	1	1	0	1	off	off	on	energised	energised
7	1	1	1	0	on	on	off	de-energised	de-energised
8	1	1	1	1	on	on	off	de-energised	de-energised

Circuit Description (Fig. 1)

Fig. 1 is a circuit diagram of the UN23/533. The unit uses positive logic throughout; the logic elements are NAND-gates.

Logic input signals are applied to pins PLA2, PLA3, PLA4 and PLA5 in accordance with Table 1. Pins PLA6, PLA7 and PLA8 are normally held at a logic 1 state. The action of relays RLA and RLB and the indication lamps is also shown in Table 1.

The relay coils and the lamps form the collector loads of transistors. A positive signal, logic 1, on the base of a transistor energises the associated relay or lamp.

If relay RLA is energised, a momentary logic 0 signal must be applied to PLA8 to release the relay. If logic 0 signals are present at PLA2, PLA3, PLA4 and PLA5, relay RLB is not normally energised. A logic 0 momentarily applied to PLA7 causes the relay to be energised and a subsequent logic 0 signal applied to PLA6 resets the relay to its de-energised condition.

Test Schedule

Apparatus Required

+12 volts Stabilised Power Supplier
+6 volts Stabilised Power Supplier
+5 volts Stabilised Power Supplier.

Test Procedure

1. Connect PLA2 to chassis.
2. Check that the Tx C/O and Main Feed lamps are on.
3. Operate the Res. Feed reset pushbutton switch and check that the Res. Feed lamp lights.
4. Set up the conditions shown in line 1 of Table 1. Connect a pin to chassis for a logic 0 input or leave the pin open-circuit for a logic 1 input. Ensire that pin PLA2 is the last to be connected.
5. Check that the resultant action corresponds to that shown in the table.
6. Momentarily connect PLA8 to chassis to reset RLA.
7. Repeat steps 4 and 5 for the other lines of the table. Use the Main Feed and Res. Feed reset pushbuttons when necessary.

Reference

Designs Department Specification 11.100(70).

Reference to Typical Associated Equipment

Television Automatic Monitor MN2M/518.

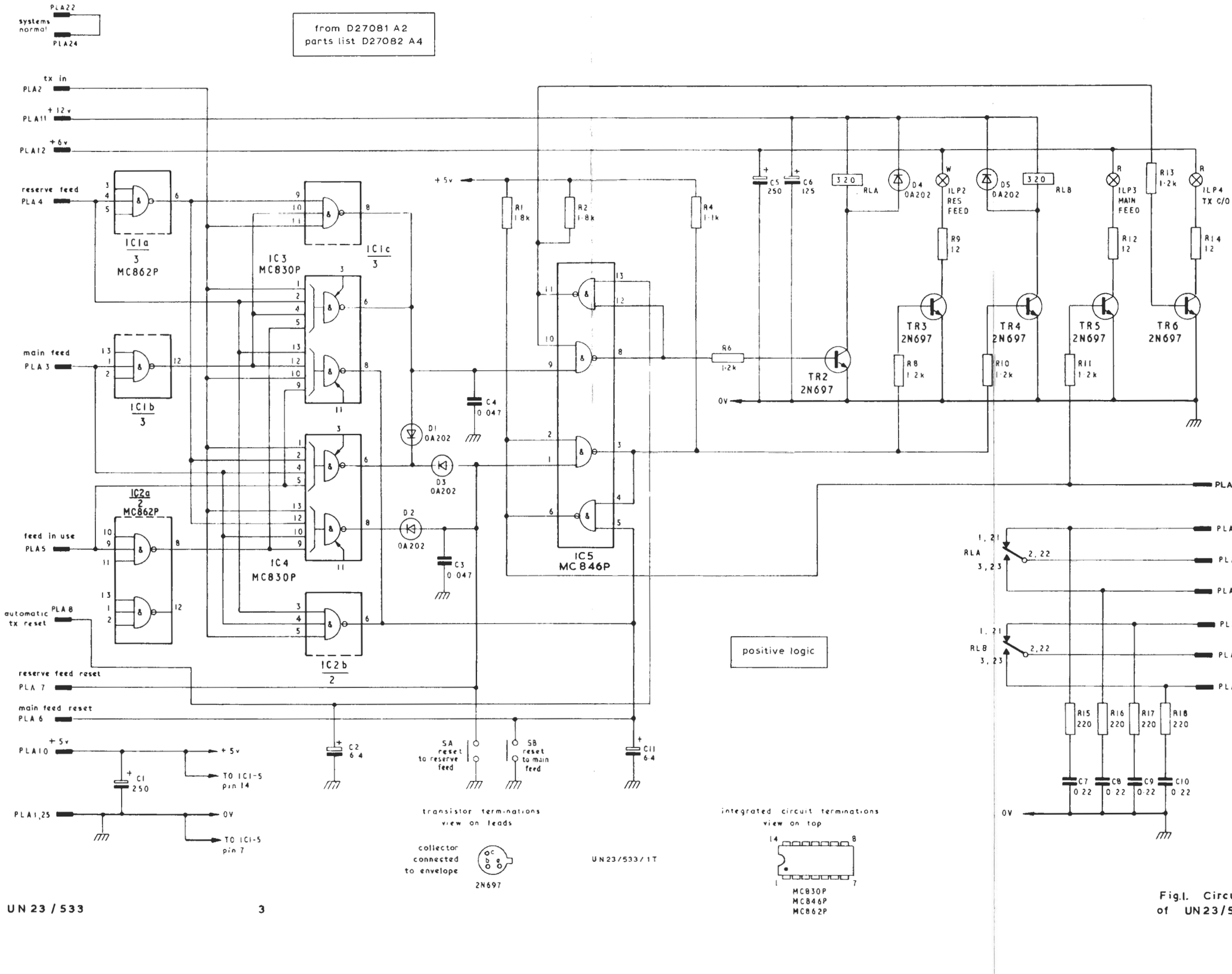

Fig.1. Circuit of UN23/533