LOGIC UNIT UN23/534

Introduction

The UN23/534 accepts d.c. logic input signals and combines and decodes these to provide d.c. logic output signals. The unit also provides three stabilised d.c. reference voltages. The UN23/534 is designed to be used in conjunction with a Television Automatic Monitor MN2M/518.

The unit is built on a printed wiring board mounted in an ISEP assembly with index pegs in positions 9, 17 and 23.

General Specification

Nominal input voltage	+5 volts d.c.
Nominal output voltage	+5 volts d.c.
Output resistance	15 ohms.
D.C. reference outputs	+5 volts, adjustment, at 5 mA maximum
	+2 volts ±100 mV at 5 mA maximum
	+2 volts ±100 mV at 5 mA maximum
Logic levels	
Logic 1	2·6 volts minimum
Logic 0	0·4 volt maximum
Pin connections	33-way ISEP plug.

Circuit Description (Fig. 1)

The circuit can be divided into three sections which are described separately.

(a) Logic Interface

Logic inputs are applied, in two groups, to pins PLA3, 4 and 5 and to pins PLA6, 7 and 8. One or more logic 1 signals, +5 volts d.c., applied to any of these inputs causes a transistor, TR1 to TR6, to conduct and present a logic 0 to the associated input of dual NAND-gate IC1 and hence a logic 1 output at pin PLA20 or PLA21.

(b) Feed Logic

A logic 1 signal is developed at PLA15 in accordance with Table 1.

(c) D.C. References

TR8 is the series element of a simple stabiliser. Variations in voltage across R14 are amplified by TR7 the output of which controls TR8, thus providing a constant current to the reference element, zener diode D1. Three outputs are derived via emitter-followers TR9, TR10 and TR11. The five-volt output at PLA27 can be adjusted by R15.

Maintenance

(a) The logic interface circuit is checked by ascertaining that a +5-volt signal at pin PLA20 or PLA21 is obtained only if one or more of the associated group inputs are at +5 volts.

(b) The feed logic circuit is similarly checked by setting up the inputs in accordance with Table 1.

(c) The procedure for checking the d.c. reference circuit is as follows:

1. Adjust R15 so that the voltage measured between PLA27 and chassis is +5 volts ±100 mV. A three-kilohm load on this supply must not reduce the output voltage by more than 50 mV.
2. Check that the voltage measured between PLA28 and chassis is +2 volts ±100 mV. Resistor R19 can be selected to achieve this requirement. A three-kilohm load on this supply must not reduce the output by more than 50 mV.
3. Check that the voltage measured between PLA29 and chassis is +2 volts ±100 mV. A three-kilohm load must not reduce the output voltage by more than 50 mV.

TABLE 1

Inputs						*Output*
PLA 11	*PLA 12*	*PLA 14*	*PLA 30*	*PLA 31*	*PLA 32*	*PLA 15*
0	0	1	0	1	1	0
0	1	1	0	1	1	0
any other inputs						1

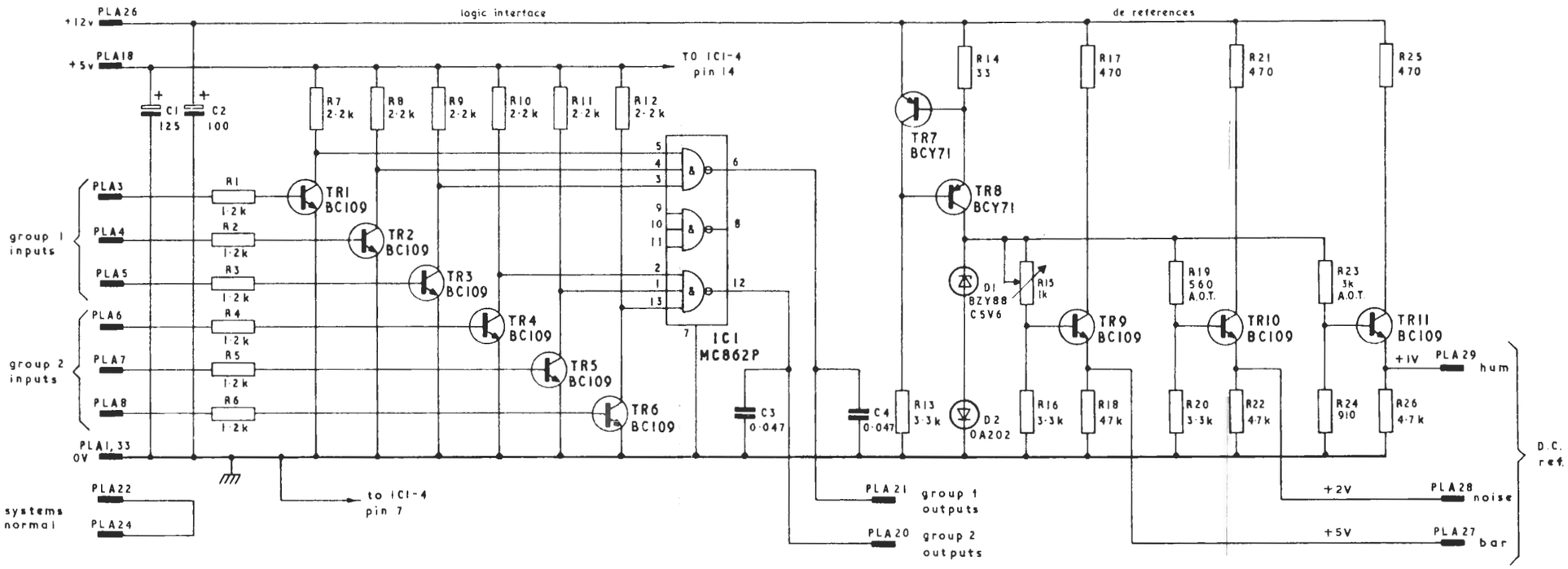
Reference

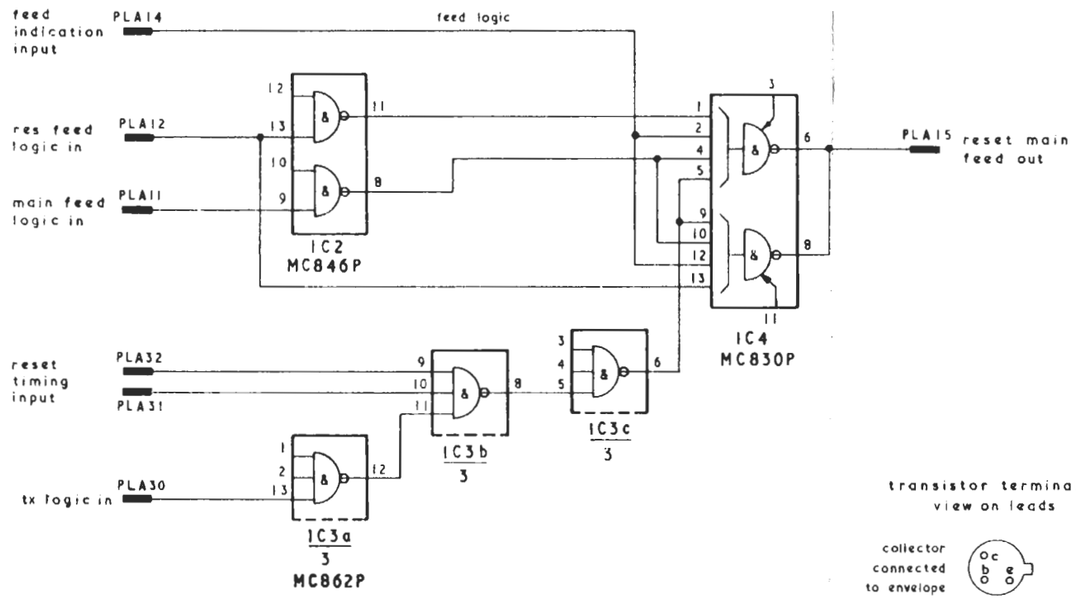
Designs Department Specification 11.105(70).

Reference to Typical Associated Equipment

Television Automatic Monitor MN2M/518.

LPB 10/72





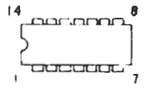
positive logic

from D27882 A2
parts list D27883 A4

transistor terminations
view on leads

BC109
BCY71

integrated circuit terminations
view on top



MC830P
MC846P
MC862P

Notes
IC2 pins 1-6 not used

Fig.1. Circuit of UN23/534