CENTRAL CONTROL UNIT UN3/12A

Introduction

The UN3/12A was designed as part of the Automatic Fault Reporter PA2M/7A. The unit accepts various input signals and provides outputs which are used to operate other units in the fault reporter.

The control unit is built on a printed wiring board which is mounted on a CH1/18C chassis with index pegs in positions 6 and 41.

Indicator lamps and switches are fitted to the front panel of the UN3/12A. Identification labels associated with these items are fitted on the front panel of a Peripheral Control Unit UN3/13A. This latter unit is always mounted adjacent to the UN3/12A.

Circuit Description (Fig. 1)

General.

The various sections of the unit are indicated on the circuit diagram, Fig. 1, and are described under separate headings below. The unit uses emitter-coupled logic circuits which operate in a positive logic convention. The logic levels are:

logic 0 – equal to or more negative than −1·7 volts with respect to chassis

logic 1 – equal to or more positive than −0·7 volts with respect to chassis.

The integrated circuit packages have been arranged on the printed wiring board for ease of manufacture. This has meant that certain inputs and outputs on circuits IC3, IC7-IC12 and IC14 have been given functions complementary to those specified by the maker. Table 1 shows the differences.

Two-second Pulse Generator

Transistors TR23 and TR24 form an emitter-coupled monostable circuit. Normally TR23 is cut off and TR24 is saturated. When the 2-kHz voltage is developed across the tuned circuit C20 and L1, transistor TR23 is saturated and TR24 is cut off. The drain voltage of transistor TR24 rises to about 0·7 volt positive and TR24 remains off for about two seconds, this time being determined by C22 and R40. During this two-second period, transistor TR25, which is normally off, is saturated; TR26 is cut off and pin PLA 1 is switched to earth potential. When TR24 conducts, transistor TR23 remains on. At the end of the timed period, TR26 switches on and a positive-going pulse is generated at the junction of R45 and R46. This pulse is applied to the clock input of the first stage of counter circuit IC7.

Dialling Mode Control Circuit

This circuit comprises IC3 and transistors TR4 and TR5. Circuit IC3 is an RS bistable device. Normally the Q output of IC3 is at logic 0, transistor TR4 is conducting and TR5 is cut off. If a logic 1 signal is applied to pin PLA4, the bistable circuit is set and changes state, and transistor TR5 is saturated. A relay in another unit[2] is connected to pin PLA5 and is energised. The bistable circuit is reset to the initial state upon receipt of a logic 1 signal from circuit IC5.

12-second Delay Circuit

Transistor TR3 is normally saturated. A logic 0 signal, −4 volts at the junction of resistors R5 and R6, is applied to the set-input of circuit IC2. When transistor TR5 switches on, diode D3 is reverse-biased and TR3 begins to cut off. Cut-off is delayed by the action of capacitor C9. After about 12 seconds the drain voltage rises sufficiently to give a logic 1 potential at the junction of R5 and R6, and circuit IC2 is set.

TABLE 1

Circuit		Pin Number							
		1	4	5	6	7	8	9	10
IC7-IC11: MC358G	Maker's designation	R	$\overline{Q}$	Q	S	$\overline{J}$	$\overline{J}$	$\overline{K}$	$\overline{K}$
	Function in UN3/12A	S	Q	$\overline{Q}$	R	$\overline{K}$	$\overline{K}$	$\overline{J}$	$\overline{J}$
IC3, IC12 and IC14: MC352G	Maker's designation		$\overline{Q}$	Q	S	S		R	R
	Function in UN3/12A		Q	$\overline{Q}$	R	R		S	S

Track-four Amplifier

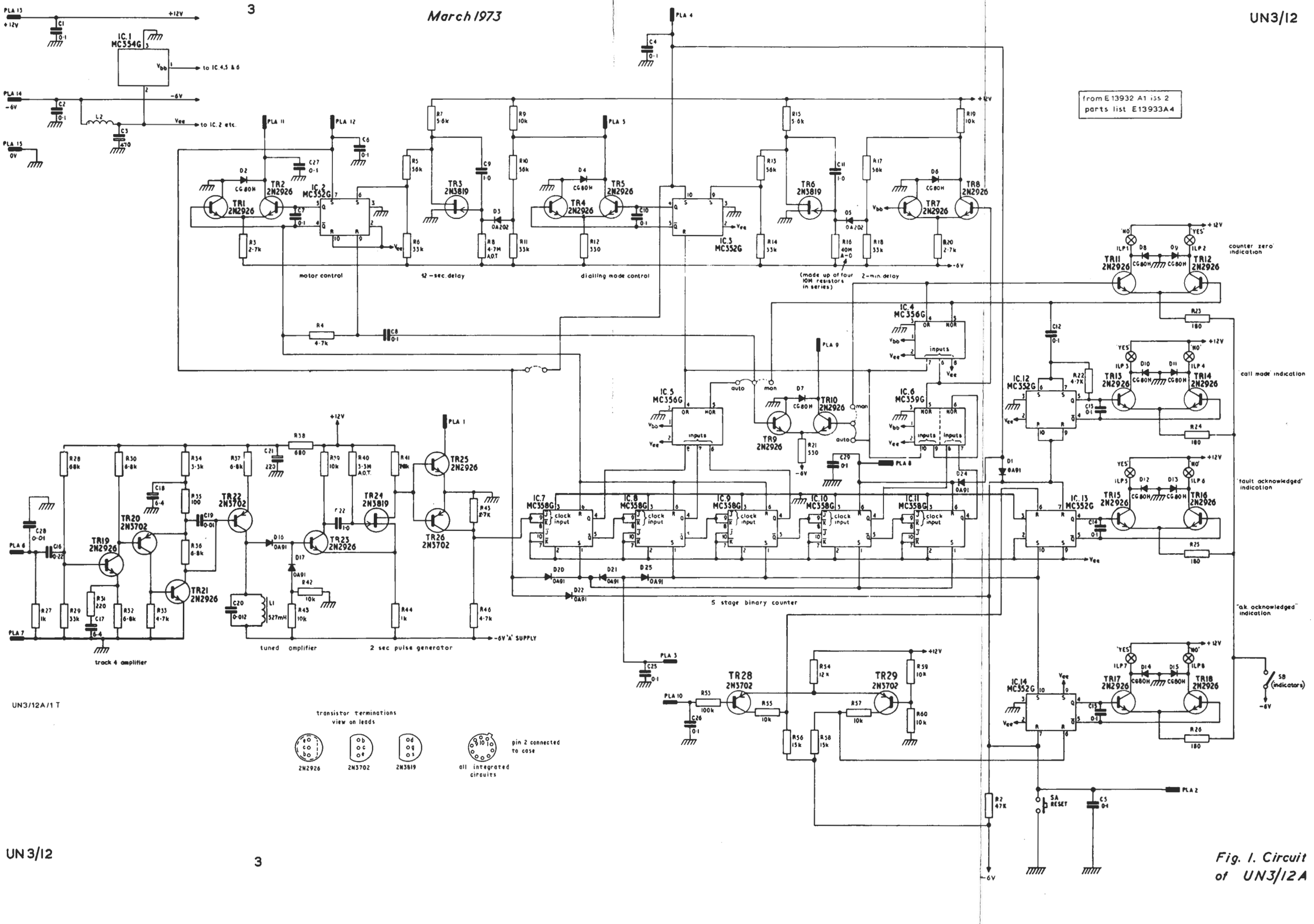
The track four amplifier comprises transistors TR19, TR20 and TR21. The output from a tape-reproducing head in another unit[1] is connected to the input at PLA6. Capacitor C19 is included to limit the gain at high-frequencies. The gain at about 2·5 kHz is reduced by 3 dB with respect to the mid-band gain.

Tuned Amplifier

The tuned amplifier TR22 is common-emitter connected with a resonant circuit as the collector load. Its input from the track-four amplifier consists of bursts of 2-kHz tone which develop a potential of 10 volts p-p across the tuned circuit.

Motor Control Circuit

The motor control circuit comprises IC2 and transistors TR1 and TR2. Circuit IC2 is an RS bistable. Initially the Q output of IC2 is at logic 0, transistor TR1 is conducting and TR2 is cut off. A logic 1 signal applied to either set input on the bistable circuit changes the state of the circuit; transistor TR2 conducts and pin PLA11 is switched to earth potential.



UN3/12A/1 T

Fig. 1. Circuit of UN3/12A

If a ring pulse is received at pin PLA12, circuit IC2 is set as before and the first, fourth and fifth stages of the counter are set, equivalent to a count of 25. A logic 1 signal is put to circuit IC5, the OR output of which is connected to the base of TR10. Transistor TR10 is saturated and pin PLA9 is switched to earth potential.

Two-minute Delay Circuit

When the counter is set to a binary count of eight, 16 or 24, the Q outputs of circuits IC7, IC8 and IC9 are all at logic 0 and the Q output of either circuit IC10 and/or IC11 is at logic 1. Circuit IC6 is a dual NOR gate, one section of which is fed with the output of circuit IC5. If the Q outputs of IC7, IC8 and IC9 are all at logic 0, the output from IC5 is logic 0. If the Q output of IC10 and/or IC11 is at logic 1, the output from the associated gate in IC6 is at logic 0. Therefore a logic 1 signal is applied to the base of transistor TR8. Transistors TR6, TR7 and TR8 are connected in a circuit similar to that used in the 12-second timer; the delay time is about two minutes. After the timed delay, circuit IC3 is set, and the fault reporter goes into the dialling mode again.

Five-stage Counter

The counter comprises five JK-bistable units, IC7 to IC11, which have a total count of 31. Table 2 shows the state of the Q output for each stage for certain numbers which are significant in the operation of the fault reporter.

Fault Acknowledged and O.K. Acknowledged Indicators

This part of the circuit comprises integrated circuits IC13 and IC14 and transistors TR28 and TR29.

In the normal condition pin PLA10 is at about +2 volts and in the fault condition at about +10 volts.

(a) Normal Condition

Pin PLA10 is at +2 volts, transistor TR28 is saturated and TR29 is cut-off. A logic 1 signal, from the junction of R55 and R56, is applied to the reset input of circuit IC13. A logic 0 signal, from the junction of R57 and R58, is applied to the reset input of IC14.

When an acknowledgement pulse, logic 1, occurs at pin PLA3, it is applied through diode D25 to the set inputs of circuits IC13 and IC14. The pulse to IC13 has no effect, but that to IC14 causes the bistable to change state.

The outputs from IC14 are connected to TR17 and TR18. After the acknowledgement pulse has been received, TR18 is saturated and an *OK. Ack. – Yes* lamp, ILP7, lights. TR17 is cut off.

(b) Fault Condition

Pin PLA10 is at +10 volts, transistor TR28 is cut off and TR29 is saturated. Logic 1 is applied to the reset input of circuit IC14; the reset input of IC13 is at logic 0. Logic 1 applied to pin PLA3, causes IC13

TABLE 2

	Q Outputs				
	IC7	*IC8*	*IC9*	*IC10*	*IC11*
	2^0	2^1	2^2	2^3	2^4
Decimal Number	*Binary Number*				
0	0	0	0	0	0
1	1	0	0	0	0
8	0	0	0	1	0
9	1	0	0	1	0
16	0	0	0	0	1
17	1	0	0	0	1
24	0	0	0	1	1
25	1	0	0	1	1
31	1	1	1	1	1

to change state. Transistor TR15 saturates and TR16 cuts off thus, lighting a *Fault Ack. – Yes* lamp.

Call Made Indicator

This circuit comprises integrated circuit IC12 and transistors TR13 and TR14. IC12 is capacitively coupled to the NOR output of IC4. Normally, TR13 is cut off and TR14 is saturated. After the fault reporter has made four attempts to dial out, the counter changes state from 31 to zero. The NOR output of IC4 then changes from logic 0 to logic 1, thus causing IC12 to change state and TR13 to saturate. The *Call Made – Yes* lamp, ILP3, lights.

Counter Zero Indication

Transistors TR11 and TR12 are connected to the outputs of circuit IC4. The arrangement is such that TR11 is cut off and TR12 is saturated only when the counter is at zero; thus a *Counter Zero – Yes* lamp, ILP2, lights.

Indicators Switch and Reset Button

The Indicators switch is used to switch the front panel lamps on and off. The lamps are normally left off to reduce battery consumption in the event of a mains failure.

The Reset button, SA, is used to light the *Call Made – No, Fault Ack. – No* and *O.K. Ack. – No* lamps.

Test Procedure

The UN3/12A is tested as part of its parent equipment.

References to Typical Associated Equipment

1. Tape Reproducer RP4/3.
2. Telephone Unit UN10/11.

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