PERIPHERAL CONTROL UNIT UN3/13A

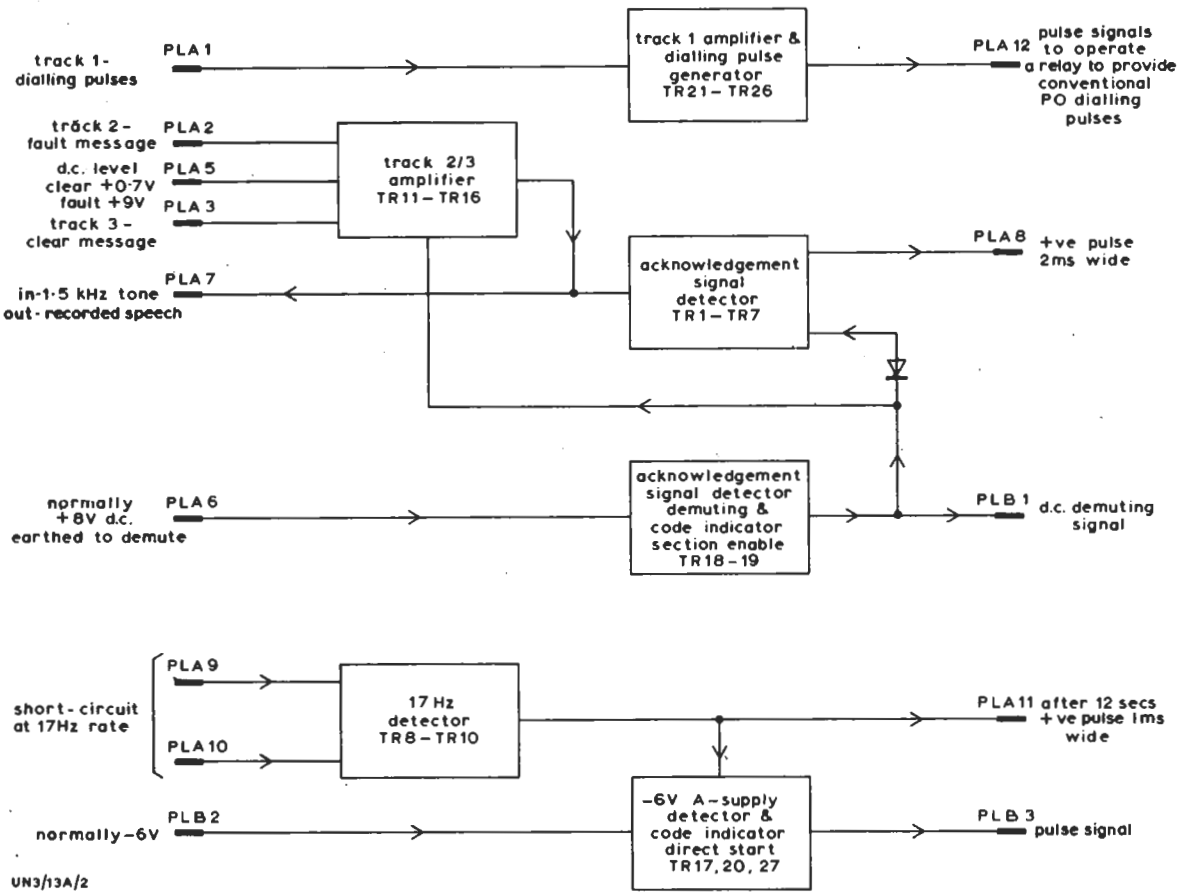


Fig. 1. Block Diagram of the UN3/13A

Introduction (Fig. 1)

The UN3/13A was designed as part of the Automatic Fault Reporter PA2M/7A. The unit has six functions. See Fig. 1.

(a) Acknowledgement Signal Detector

The acknowledgement signal detector circuit accepts audio frequency signals; if a prolonged 1·5-kHz component is present a 2-ms positive-going pulse is generated.

(b) 17-Hz Detector

The 17-Hz detector circuit accepts a 17-Hz telephone ringing signal through the contacts of a relay in an associated unit[1]. A single 1-ms positive-going pulse is generated.

(c) Track-2/3 Amplifier

This circuit comprises a tape reproducing amplifier fed from two reproducing heads on an associated machine[2].

(d) Track-1 Amplifier and Dialling Pulse Generator

Telephone dialling pulses, in the form of bursts of 2-kHz tone, are fed from a tape reproducing head in another unit[2] to the track-1 amplifier. The output of the amplifier triggers a pulse generator which produces d.c. signals to operate a relay in an associated unit[2]. The opening and closing of the relay contacts operates Post Office telephone exchange equipment.

(e) Acknowledgement Signal Detector Demuting and Code Indicator Section Enable

This circuit demutes the Acknowledgement Signal Detector (a) at a predetermined time and prepares other circuits[3,4] for subsequent operation.

(f) Negative 6-volt A-supply Failure Detector and Code Indicator Direct Start

This circuit detects the interruption of the negative six-volt A supply and prepares other circuits[4] for subsequent operation.

The unit is constructed on three printed wiring boards which are mounted on a CH1/18C chassis. Index pegs are fitted in positions 48 and 55.

Engraving on the front panel of the unit refers to indication lamps on a Central Control Unit UN3/12A. The UN3/12A and the UN3/13A are always adjacently mounted.

Circuit Description (Fig. 2)

Fig. 2 is a circuit diagram of the unit. All signal levels in the following description are referred to the standard zero level of 0·775 volt across 600 ohms.

(a) Acknowledgement Signal Detector

Transistors TR1, TR2 and TR3 form an amplifier with a gain of about 34 dB for signal levels below −40 dB. Diodes D1 and D2 conduct on peak voltage levels above −40 dB. The feedback path provided limits the level variation at the amplifier output (TR3 collector) to about 4 dB for input signals within the range −40 to 0 dB.

Transistor TR4 is normally saturated because its base resistor, R11, is taken to the 12-volt positive rail. During a specified acknowledgement gap transistor TR4 is cut-off, see Circuit Description (e), and the output of the amplifier is applied to a series tuned circuit, L1C4, which resonates at 1·5 kHz. If the frequency of the signal applied to TR1 contains a substantial 1·5-kHz component, an alternating potential of about 10 volts p-p is developed across L1. Diode D4 rectifies this signal and a charge begins to build up across capacitor C5. Transistor TR5, which in the absence of an input signal is saturated, starts to cut off. Capacitor C6, connected from drain to gate of TR5, slows down the rate of cut-off. The value of resistor R12 is chosen so that TR5 cuts off about 500 ms after capacitor C5 has been fully charged. When TR5 is cut off, TR7 also cuts off and its collector potential moves towards the six-volt negative rail. When the collector reaches one volt negative, transistor TR6 begins to conduct and its own collector potential rises from six volts negative to about 0 volts. This change, which is a positive feedback action, is fed to the base of TR7, through capacitor C7, to ensure that TR7 cuts off quickly. When TR7 cuts off, a positive-going pulse is produced at pin PLA8. The collector of TR6 rises to almost zero volts, diode D5 is forward-biased, TR5 and TR7 bottom again and TR6 is cut off. The width of the output pulse is about 2 ms.

(b) 17 Hz Detector

A 17-Hz ringing signal to the parent equipment causes a relay to open and close across PLA9 and PLA10. This produces an 18-volt p-p square-wave at the junction of R18 and C9. The square-wave is converted to a positive-going staircase waveform across capacitor C10. Components C9, C10, D7 and D8 form a conventional diode-pump circuit.

Transistors TR8 and TR9 form an emitter-coupled monostable multivibrator. Normally TR8 is cut-off and TR9 is saturated. The potential at the emitter of TR8 is arranged to be more positive than that at its base. After a few cycles of the input signal the voltage across capacitor C10 causes transistor TR8 to switch on and TR9 to be cut off. The drain potential of TR9 rises to 12 volts positive. After about 12 seconds, transistor TR9 is saturated again. The delay time is determined by components R22, R23 and C11. The drain potential of TR9 goes negative to cause transistor TR10 to saturate for about 1 ms. The output at pin PLA11 is a 1-ms positive-going pulse.

(c) Track-2/3 Amplifier

Outputs from tracks two and three of an associated tape machine[2] are fed to pins PLA2 and PLA3 respectively. A direct voltage, dependent upon the state of monitored conditions in the parent unit, is applied to pin PLA5. There are two conditions (a) Clear:– when the voltage is +9 and (b) Fault:– when the voltage is +0·7. These potentials are developed in another unit[5]. With a Clear input, transistor TR12 is saturated and TR11 is cut off. The input signals from the tape machine are passed via the saturated transistor to a three-stage amplifier comprising TR13, TR14 and TR15. The amplified signal is applied to the base of transistor TR16, whose collector load is a transformer in a separate unit[1]. The gain and hence the audio output of this stage can be varied by means of resistor R47 in the emitter circuit of TR16. Diode D15 is forward-biased during the acknowledgement gap and mutes the amplifier, see Circuit Description (e). This ensures that noise on the tape and in the amplifier is reduced and does not cause spurious operation of the acknowlegement detector.

(d) Track-1 Amplifier and Dialling Pulse Generator

An input corresponding to track 1 of the associated tape machine is fed to pin PLA1. The input comprises dialling pulses in the form of bursts of 2-kHz tone. The tone bursts are amplified by a three-stage amplifier, comprising transistors TR21, TR22 and TR23. The amplifier is similar in form to that used for the Track-2/3 Amplifier described in (c). The output, at the collector of TR23, is fed to the base of transistor TR24 which forms a single-stage tuned amplifier. Components L2 and C36 resonate at 2 kHz. When the tone bursts are replayed the voltage developed across L2 and C36 is about 10-volts p-p.

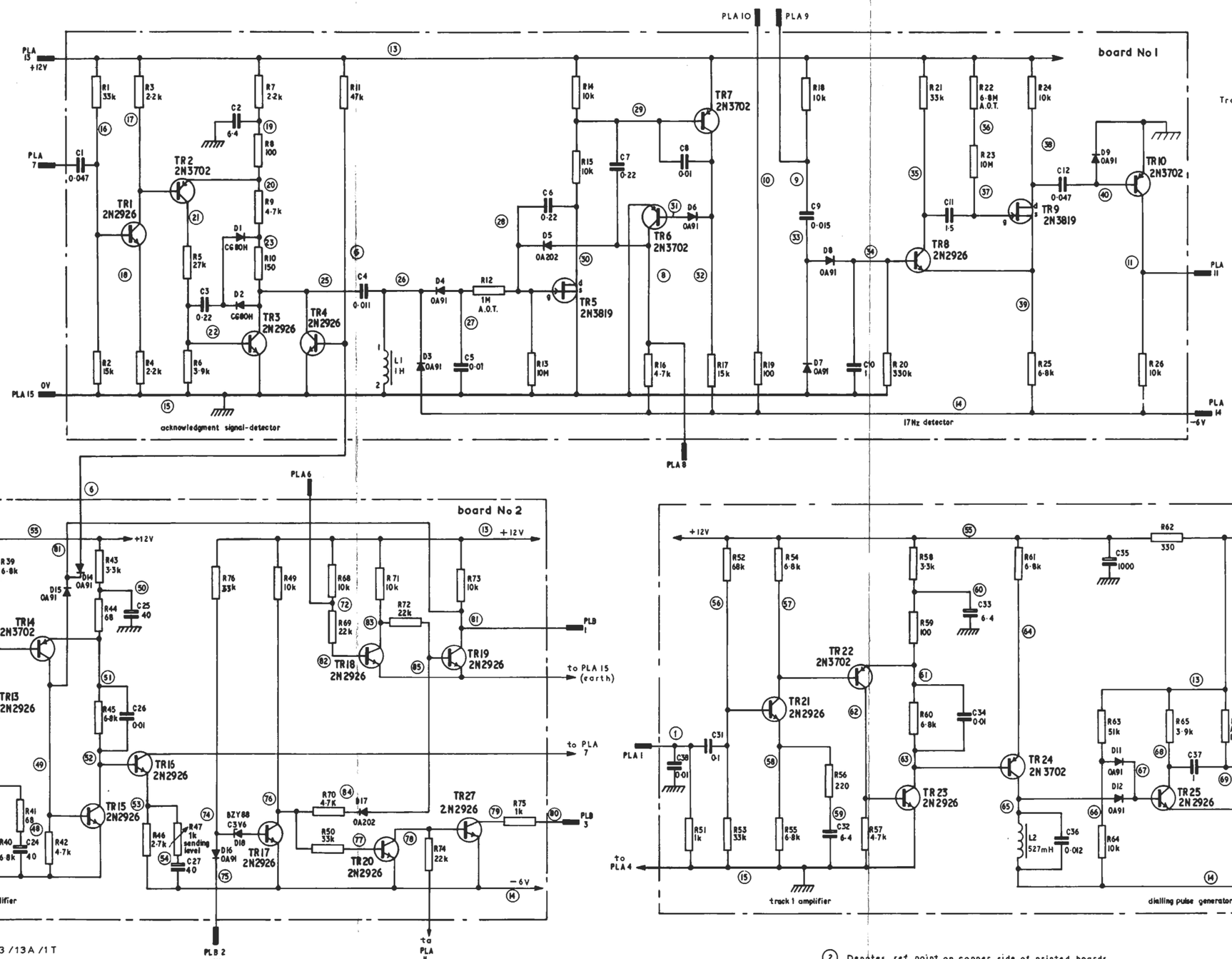
Transistors TR25 and TR26 form an emitter-coupled monostable multivibrator. The collector of TR26 is taken to a positive 12-volt supply via a dialling relay coil in another unit[1]. Normally transistor TR26 is saturated and TR25 is cut off. The positive voltage peaks developed across the tuned circuit cause transistor TR25 to saturate, TR26 to cut off and the dialling relay to be de-energised. Transistor TR26 remains off for 67 ms, after which the relay is energised again.

(e) Acknowledgement Signal Detector Demuting and Code Indicator Section Enable

A positive eight-volt supply from another unit[6] is connected to pin PLA6. The potential remains at this value during standby conditions or while the associated tape machine is being played. Transistor TR18 is saturated and transistor TR19 is cut off. During the acknowledgement gap period an earth is connected to pin PLA6 causing TR18 to cut off and TR19 to saturate. The collector potential of TR19 forward-biases diodes D14 and D15 and causes transistors TR4 and TR15 to cut off, see Circuit Description (a) and (c).

Three actions take place during the acknowledgement gap period:

(a) The Acknowledgement Signal Detector is demuted.



UN3/13A/1T

(2) Denotes ref point on copper side of printed boards

Fig. 2. Circuit of UN3/13A

(b) The Track-2/3 Amplifier is muted.
(c) Logic circuits in another unit[4] are enabled by the potential at pin PLB1.

(f) Negative Six-volt Supply Failure Detector and Code Indicator Direct Start

Under normal conditions a six-volt negative supply is connected to pin PLB2. Diode D16 is forward biased and the voltage drop across resistor R76 and across zener diode D18 is such that transistor TR17 is cut off. Diode D17 is reverse-biased.

Transistor TR20 draws base current through resistors R49R50. TR20 and TR27 are cut off because pin PLA11 is at −6 volts. The collector of transistor TR27 is taken to a zero-volt rail in another unit. Pin PLB3 is at zero volts.

If the six-volt supply at PLB2 fails, transistor TR17 conducts. The supply failure causes pin PLA6 to rise to zero volts and TR18 conducts. Transistor TR19 would also conduct, but diode D17 is forward-biased and TR19 and held off.

If, when the six-volt supply is normal, an incoming ring is detected, TR20 conducts; TR10 is switched on and pin PLA11 is switched to zero volts. Transistor TR27 is held off because the saturated TR20 is connected across its base and emitter. Pin PLB3 is held at zero volts.

If the six-volt supply has failed and an incoming ring is detected, TR20 is held off. This is because TR17, connected across the base and emitter of TR20, is saturated. TR27 is saturated and pin PLB3 is switched to −5 volts for a few milliseconds.

Maintenance

General

So called 'node numbers' are printed on the copper side of each printed wiring board and are shown in Fig. 2. The d.c. potential at each node, measured under prescribed conditions, is given in Table 1. All voltages are with respect to PLA15.

Measuring Conditions

1. Connect a +12-volt supply to PLA13, negative to PLA15.
2. Connect a −6-volt supply to PLA14, positive to PLA15.
3. Connect PLA5 to PLA13.
4. Connect PLA14 to PLB2.
5. Connect a 47-kilohm resistor from PLA13 to PLB3.
6. Connect a 24-kilohm resistor from PLA13 to PLB1.

References to Typical Associated Equipment

1. Telephone Unit UN10/11.
2. Tape Reproducer RP4/3.
3. Scan Unit UN1/98.
4. Scan Control Unit UN3/16.
5. Input Logic Delay Unit UN14/4.
6. Central Control Unit UN3/12A.

TABLE 1

	Node	Voltage	Node	Voltage	Node	Voltage
Board No. 1	6	0·6	19	8·4	29	11·4
	8	−6·0	20	8·2	30	0·3
	9	12	21	0	31	
	10	−6·0	22	0	32	11·8
	11	−6·0	23	0·3	33	0
	13	12	24	0·1	34	0
	14	−6·0	25	0·1	35	12
	15	0	26	0	38	1·3
	16	3·6	27	0	39	1·2
	17	9·1	28	0	40	0
	18	3·2				
Board No. 2	2	0	47	3·3	75	−6.0
	3	0	48	3·3	76	7·5
	5	12	49	−0·5	77	−5·4
	6	0·6	50	6·6	78	−5·9
	14	−6·0	51	6·5	79	0
	15	0	52	−1·1	80	0
	41	5·0	53	−1·7	81	12
	42	4·4	54	−1·7	82	0·6
	43	3·8	55	10·6	83	0·05
	44	0	72	8·0	84	7·5
	45	3·8	73	7·0	85	0·05
	46	7·3	74	−5·7		
Board No. 3	12	−4·9	58	2·8	65	−6·0
	13	12	59	2·8	66	−3·8
	14	−6·0	60	8·6	67	−4·0
	15	0	61	−8·5	68	−4·5
	55	10·5	62	0·6	69	−4·7
	56	3·0	63	5·0	70	−4·1
	57	7·5	64	5·6	71	−4·7