SCAN CONTROL UNIT UN3/16

Introduction

The UN3/16 is designed together with the UN1/98 as part of the code indicator section of the Automatic Fault Reporter PA2M/7A. The two units perform between them a function similar to that of a Telephonic Indicator Panel TIP/2.

The UN3/16 is built on a BBC/I.S.E.P. printed wiring board with connections made via a 33-way I.S.E.P. connector on which segments 3, 5 and 17 are removed from the coding device.

General Data

Logic levels, 1	−2·5 to 0 volts
0	−4·2 to −5·5 volts
Frequency of output tone	1·2 kHz
Tone output level	−5 dBm
Programme output level	+3 dBm peak
Power requirements	−6 volts
	+12 volts

Circuit Description (Figs. 1 and 2)

In what follows, each item on block diagram Fig. 1 is described separately.

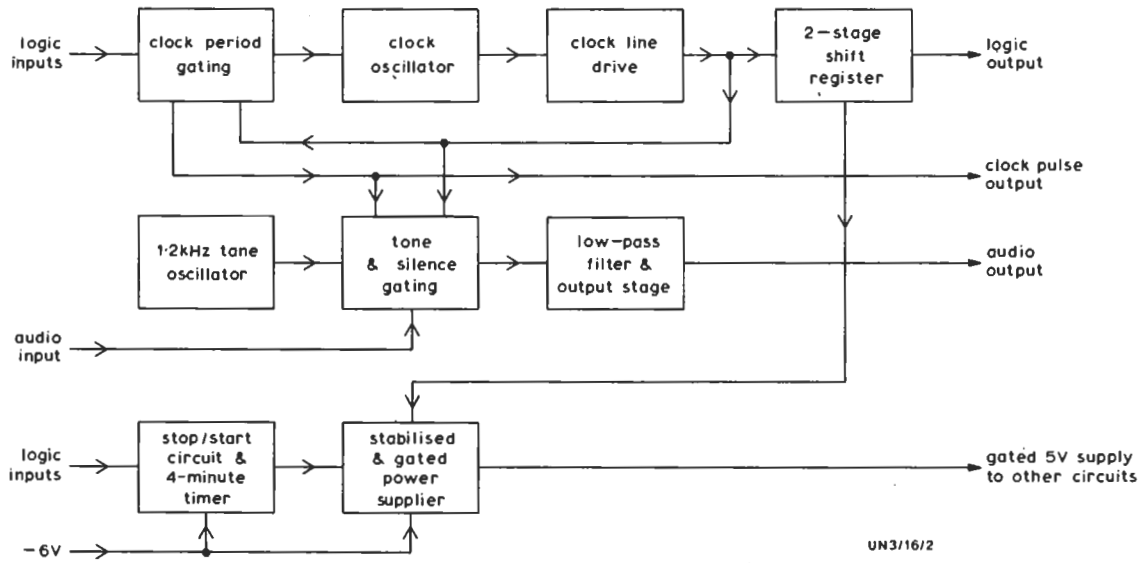

Fig. 1. Block Diagram of the UN3/16

Stabilised and Gated Power Supplier

This comprises TR9 to TR13, arranged to form a conventional shunt/series stabiliser. The unstabilised input, six volts negative, is applied to PLA32. A five-volt negative supply is obtained from the emitter of TR11 to power the stop/start circuit and the four-minute timer. All other circuits are fed with a five-volt negative supply from TR13 emitter; this supply can be cut off by applying logic 0 to TR12 base which in turn cuts off TR13.

Four-minute Timer

The timer circuit comprises TR22 to TR24. In the static state, logic 0 is applied to R51 at the input to the timer, timing capacitors C14 and C15 are discharged through R54 and D8, and the transistors are cut off.

To start a timing sequence, logic 1 is applied to the input on PLA30. When a positive-going acknowledgement pulse is applied to PLA33, circuit IC8 changes state. The timing capacitors then begin to charge. After about four minutes, the base of TR22 reaches the emitter potential and the transistor begins to conduct. At the same time, TR23 also begins to conduct and the positive-going transition at its collector is fed back to TR22 base, thus increasing the conduction of TR22. When TR23 bottoms, TR24 also bottoms and logic 0 is applied to a bistable element, IC8, in the stop/start circuit. A logic 0 output from IC8 to the input of the timer causes the timing capacitors to discharge and the circuit resumes its static state.

Stop/Start Circuit

This circuit comprises TR14 to TR16 and IC8. In the initial state, the Q output of IC8 is at logic 0, the four-minute timer is discharged and the gated five-volt supply is off.

A logic 1 signal on PLA27 and PLA30 causes TR16 and TR14 to be cut off and saturated respectively and logic 1 is applied to the S1 input of IC8.

If logic 1 is applied to PLA33, TR15 saturates and the positive transition at its emitter is applied to the clock pulse input of IC8. The Q output of IC8 changes to a logic 1 and causes the gated five-volt supply to be switched on and start the timer.

After the timed period, a logic 0 signal is applied to the C_D input of IC8. This resets the Q output to logic 0, switches off the gated five-volt supply and discharges the timing capacitors.

Pins PLA26 and PLA31 are connected to the S_D and C_D inputs respectively of IC8. A logic 1 signal may be applied to either of these pins to allow the sequence to be directly started or stopped. These inputs override any other inputs to IC8.

If a logic 1 pulse is applied to PLA33 when the timer is running and PLA2 is at a logic 1 level, the Q

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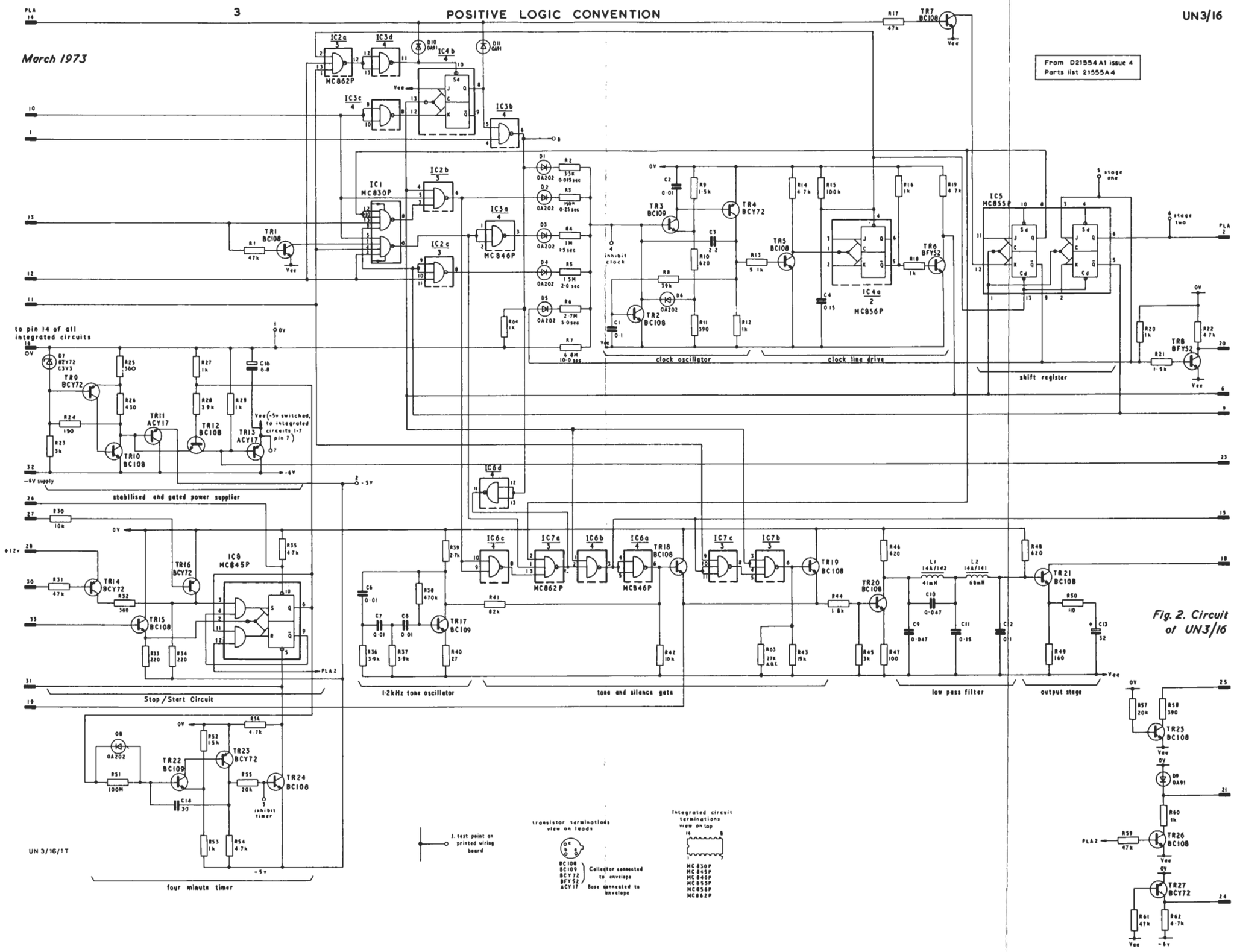

Fig. 2. Circuit of UN3/16

output of IC8 changes to logic 0 and transistor TR12 is cut off.

1·2-kHz Tone Oscillator, Low-pass Filter and Output Stage

The tone oscillator, TR17, is a conventional phase-shift oscillator with an output frequency of 1·2 kHz. The output is fed via TR20, an m-derived low-pass filter and TR21.

The filter response is shown in Fig. 3. The shape is due partly to the filter and partly to the effect of transfomers in associated units[1, 2].

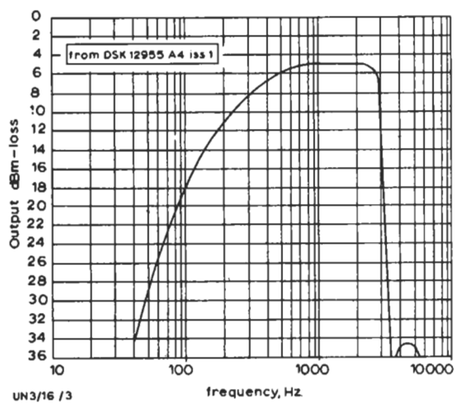

Fig. 3. Theoretical Response of the Programme Channel

Clock Oscillator and Line Drive Units

The clock pulse oscillator comprises TR2 to TR4. Timing components C3 and R7 allow a clock pulse output after 10 seconds. For shorter delays, one of the resistors R2 to R6 is connected in parallel with R7 by forward-biasing one of the associated diodes D1 to D5.

In the initial state, the transistors in the clock oscillator are not conducting. The gated five-volt supply is switched on and capacitor C3 begins to charge through the selected timing resistor, say R7. When the potential at the base of transistor TR3 becomes more positive than that at its emitter, the transistor begins to conduct. At the same time, TR4 starts to conduct and a positive feedback action through capacitor C3 ensures that both transistors are bottomed. After a short delay, determined by R8 and C1, TR2 saturates and discharges C3. Diode D6 ensures that C3 is always discharged to the same potential; this helps to maintain the accuracy of each timed period.

Clock Line Drive

TR5 is a common-emitter stage which drives IC4a/2. The Q output of IC4a/2 feeds TR6, another common-emitter stage. When the line-drive circuit is first powered, a negative-going pulse, developed across C4, is applied to the S_D input of IC4a/2; this sets the $\overline{Q}$ output to a logic 1. Each time capacitor C3 is discharged, the $\overline{Q}$ output of IC4a/2 changes to logic 0 which brings the 0·25 second timing resistor, R3, into circuit to ensure that each clock pulse is 0·25 second wide.

Shift Register

Circuit IC5 comprises two JK bistables connected to form a shift-register. Information entering the first stage at the K input is passed to the J input of the second stage by the negative-going edge of the first clock pulse. Subsequently this information is passed to the Q output by the second clock pulse. Logic 0 applied to the C_D terminals sets the Q output of each stage to logic 0, regardless of the inputs to the other terminals.

In the initial state, the register is preset by a negative-going pulse which is developed across C4 when the supply is switched on. Unused terminals, kept open-circuit, are effectively at the logic 1 state.

Table 1 shows the action of the shift register.

The register is now reset to its initial state, as shown in the first line of the table, and the sequence is repeated.

Tone and Silence Gates

TR18 and TR19 comprise the tone and silence gates respectively, these transistors are switched by the output from associated NAND-gates, and both transistors never conduct at the same time. When TR18 is conducting, the output of the tone oscillator is switched to PLA18. When TR18 is cut off, TR19 is saturated. The base of output transistor TR20 is therefore effectively earthed. If both transistors are cut off, an audio input to PLA19 is switched to PLA18. The bias on TR20 is held constant by a saturated transistor in an associated unit[1].

Operation

A typical operating sequence is as follows:

(a) A logic 1 signal is applied to PLA30 to enable the C.I.S.

(b) A logic 1 signal is applied to PLA33. The gated five-volt negative supply is switched on.

(c) A negative-going pulse is developed across capacitor C4 and used to reset circuits IC4 and IC5. The $\overline{Q}$ output of the first stage is set to logic 1. Transistor TR8 conducts. The resulting logic 0 at PLA20 is used to reset a shift register in another unit[3].

(d) Transistor TR25 is saturated and a logic 1 is applied to pin PLA25. Transistor TR27 is saturated and a logic 1 is applied to pin PLA24.

(e) Inputs on pins PLA1, 10, 11, 12, 13 and 14 are at logic 1.

(f) Diode D5 is conducting, the other diodes are cut off, and the clock oscillator timing is set to five seconds. The tone gate TR18 is conducting and the silence gate TR19 is cut-off; five seconds of tone are applied to the output on pin PLA18.

(g) After the five seconds have elapsed, a 0·25-second clock pulse occurs. Transistor TR18 is cut off and TR19 conducts. The audio output is silenced. Diode D5 is reverse-biased and diode D4 conducts to set the timer to a two-second period. Logic 0 is applied to PLA9 to enable another unit[3].

TABLE 1

Action		*1st Stage* J	K	Q	$\overline{Q}$	*2nd Stage* J	K	Q	$\overline{Q}$
Switch on (reset pulse to C_D inputs)		1	0	0	1	1	1	0	1
1st clock pulse	+ve edge								
	–ve edge	1	0	1	0	0	1	1	0
2nd clock pulse	+ve edge								
	–ve edge	1	0	1	0	0	1	0	1
3rd and subsequent clock pulses	+ve edge								
	–ve edge	1	0	1	0	0	1	0	1
Logic 1 to stage-1 K input		1	1	1	0	0	1	0	1
Next clock pulse	+ve edge								
	–ve edge	1	0	0	1	1	1	0	1

(h) After two seconds a clock pulse occurs; transistor TR18 conducts and TR19 is cut-off. Diode D4 is reverse-biased.

(i) In this condition pins PLA1, 10, 11, 12, 14 and 15 are at a logic 1 level and the clock oscillator timing depends upon the logic level applied to PLA13. A logic 1 level at PLA13 brings diode D2 into conduction and applies a 0·25-second burst of tone at the output. A logic 0 applied to pin PLA13 brings diode D3 into conduction and a 1·5-second burst of tone is applied to the output.

(j) If, during the action detailed in (i), logic 0 is applied to PLA1, diode D1 conducts. At the same time, tone gate TR18 is cut off. There is thus a silent period 0·01 second in duration.

(k) If a logic 0 is applied to pin PLA12, then assuming pins PLA1, 10, 11 and 14 are at logic 1 and pin PLA13 is at logic 0, diode D4 conducts and TR18 is cut off. A two-second silent period occurs.

(l) If a logic 0 is applied to pin PLA10, then on the following clock pulse diode D1 conducts, allowing the clock oscillator to time for 0·15 second; this condition is not changed until logic 0 is applied to PLA11 or PLA12 to reset circuit IC4b. If a logic 0 is applied to pin PLA11, diodes D1 to D5 are reverse-biased and the clock oscillator is timing under the control of resistor R7 for a period of 10 seconds. The tone is cut off but the silence gate TR19 is not conducting. An audio signal applied to pin PLA19 is passed to the output on pin PLA18.

(m) When the monitoring sequence has been completed a logic 0 is applied to pin PLA14. This applies a logic 1 to the K input of the first stage of the shift register, and the whole sequence can be repeated.

Maintenance

The UN3/16 should be tested as part of its parent unit.

References to Typical Associated Equipment

1. Scan Unit UN1/98.
2. Telephone Unit UN10/11.
3. Reset Control Unit UN3/28.