RESET CONTROL UNIT UN3/28

Introduction

The UN3/28 is designed as part of the Automatic Fault Reporter PA2M/7A. The unit accepts various logic signal inputs; when the correct combinations of inputs are present timed periods of steady or pulsed tone are generated. Six switched 12-volt supplies are provided for switching external circuits.

The unit is built on a printed wiring board which is mounted on a CH1/18C chassis. Index pegs are fitted in positions 56 and 57.

Brief Specification

Audio Output	−5 dBm into a 300-ohm load.
Switched Outputs	Zero to +12 volts for up to five seconds. Each output can deliver a maximum of 50 mA.
Power Requirements, when feeding six one-kilohm loads	+12 volts at 20 to 90 mA. −6 volts at 60 to 70 mA.
Logic Levels	
Logic 0	−4·5 to −5·5 volts.
Logic 1	0 to −1·0 volts.

Circuit Description (Figs. 1 and 2)

Fig. 1 is a block diagram and Fig. 2 the circuit diagram of the UN3/28. The unit is described in nine separate sections.

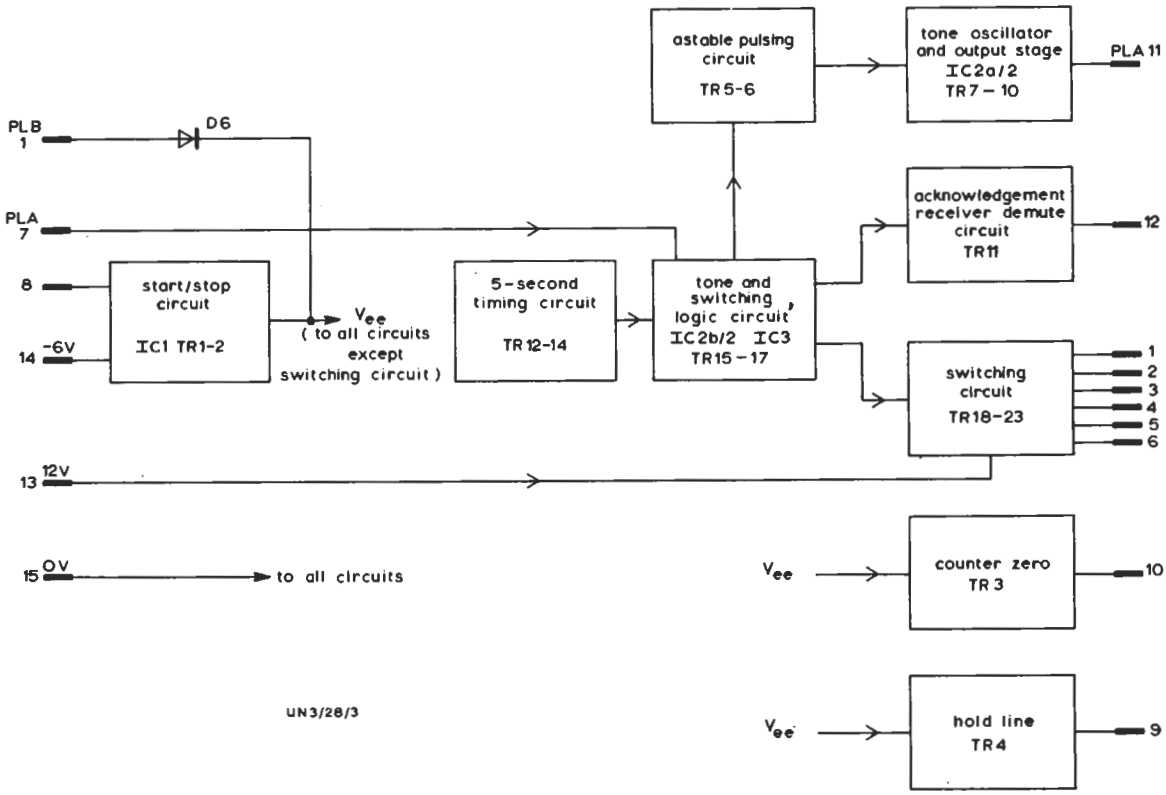

Fig. 1. Block Diagram of the UN3/28

Stop/start Circuit

This circuit comprises IC1 and transistors TR1 and TR2. Normally transistor TR2 is cut off by the application of a logic 0 to its base. When the unit is started TR2 conducts and a negative five-volt supply, V_{ee}, is made available at its collector.

In the static state a logic 1 is present at pin PLA8, a logic 0 at pin PLA7 and a logic 0, from the tone and switching logic section, at pin 13 of IC1. The unit is started by applying a logic 0 to pin PLA8 and a momentary logic 1 to PLA7. When V_{ee} is applied to the tone and switching logic section, pin 13 of IC1 changes to logic 1 and the circuit remains on. When pin 13 is changed back to logic 0 (see Table 2) the circuit switches off.

Five-second Timing Circuit

The five-second timing circuit comprises transistors TR12 to TR14. The timer is started when the negative five-volt supply, V_{ee}, is connected. Capacitor C7 charges via resistors R27 and R31. When the voltage across C7 is more positive than that at the junction of resistors R29 and R30, transistors TR13 and TR14 begin to conduct. After a short delay, determined by components C9 and R28, transistor TR12 bottoms and capacitor C7 is discharged; the cycle then repeats. The output, from the collector of common emitter amplifier TR15, is a 2-ms negative-going pulse of amplitude 5 volts p-p.

Astable Pulsing Circuit

This circuit comprising transistors TR5 and TR6 is a conventional astable multivibrator circuit. The circuit is started when the negative five-volt supply is connected.

Tone Oscillator and Output Stage

Transistor TR9 forms a conventional phase-shift audio oscillator which feeds a common-emitter

stop / start circuit | hold line circuit | astable pulsing circuit | audio oscillator | output stage

PLA15 15 0V

PLA9 9

PLA8 8

PLA14 14 -6V

PLA10

PLA13 13 12V

PLA7 7

0V

V_{ee}

IC1 MC846P OR DIC846N

IC2a/2 MC846P OR DIC846N

IC3a/2 MC846P OR DIC846N

IC3b/2

IC2b/2

TR1 BC108 — TR2 BC108 — TR3 BCY71 — TR4 BC108 — TR5 BC109 — TR6 BC109 — TR7 BC108 — TR8 BC108 — TR9 BC108 — TR10 BC108 — TR11 BC108 — TR12 BC108 — TR13 BC109 — TR14 BCY72 — TR15 BC108 — TR16 BC108 — TR17 BC108 — TR18 BCY72 — TR19 BCY72 — TR20 BCY72 — TR21 BCY72 — TR22 BCY72 — TR23 BCY72

D1 BYX22-200 — D2 0A91 — D3 0A91 — D4 0A91 — D5 BZY88 C15 — D6 0A91 — D7 0A202 — D8 0A202 — D9 0A202 — D10 0A202 — D11 0A202 — D12 0A202

R1 220 — R2 1k — R3 1k — R4 20k — R5 4·7k — R6 20k — R7 390 — R8 4·7k — R9 470k — R10 470k — R11 4·7k — R12 20k — R13 4·7k — R14 3·9k — R15 4·7k — R16 1·8k — R17 47k — R18 470k — R19 2·7k — R20 27 — R21 47k — R22 20k — R23 16k — R24 160 — R25 47k — R26 1k — R27 5·6m — R28 39k — R29 1·5k — R30 1k — R31 1k — R32 10k — R33 4·7k — R34 20k — R35 20k — R36 10k — R37 220 — R38 100k — R39 3·9k — R40 1·3k — R41 1·3k — R42 1·3k — R43 1·3k — R44 1·3k — R45 1·3k

C0 0·1 — C1 0·68 — C2 0·68 — C3 0·01 — C4 0·01 — C5 0·01 — C6 0·1 — C7 2·2 — C9 0·1 — C10 6·4 — C11 0·1 — C12 0·1 — C13 0·1 — C14 0·1 — C15 0·1 — C16 0·1 — C17 0·1

L1 30μ — L2 30μ — L3 30μ — L4 30μ — L5 30μ — L6 30μ

FS1 100mA — FS2 100mA — FS3 100mA — FS4 100mA — FS5 100mA — FS6 100mA

PLA11 11 — PLA12 12 — PLB1 16

PLA1 — PLA2 — PLA 3 — PLA4 — PLA5 — PLA6

switching circuit

From D28167A2 issue 3
Parts list D26720A4

transistor terminations viewed on leads — collector connected to envelope — BCY71 BC108 BCY72 BC109

integrated circuit terminations view on top — MC846P OR

6 numbered pin on printed wiring board

five second timing circuit | tone and switching logic

Fig. 2. Circuit of UN3/28

TABLE 1

Output	*IC2a/2 Pins*			*TR8 Base via R17*	*TR8*
	4	5	6		
tone off	0	0 or 1	1	1	conducting
f.m. tone	0	0 or 1	1	0	cut off
pulsed tone off	1	0	1	1	conducting
pulsed tone on	1	1	0	0	cut off

output stage TR10. The oscillator frequency can be changed by altering the combined value of resistors R15 and R16. This is done by switching transistor TR7 on and off, by means of the output from the astable pulsing circuit, and therefore shorting R16.

The output of the oscillator is muted when transistor TR8 conducts. This muting is done by applying suitable logic signals to IC2a/2 and to the base of transistor TR8 via resistor R17, see Table 1. The output is either five seconds of frequency modulated tone or a period of up to five seconds of pulsed tone.

Switching Circuit

Transistors TR18 to TR23 saturate when a logic 0 signal is applied to each base via diode D5. When the transistors switch on, the associated output pins PLA1 to PLA6 rise from earth potential to 12 volts positive for a period of up to five seconds.

Counter Zero

When the unit is started, transistor TR3 is saturated, and pin PLA10 rises to logic level 1.

Hold Line

When the unit is started transistor TR4 is saturated and pin PLA9 falls to zero volts. The collector load for TR4 is in another unit[1].

Acknowledgement Receiver Demute

When a logic 1 signal is applied to the base of transistor TR11, pin PLA12 falls to zero volts.

Tone and Switching Logic Circuit

The tone and switching logic circuit is drawn separately in Fig. 3. Table 2 shows the logic levels relating to the circuit for the various conditions encountered.

Test Procedure

The UN3/28 should be tested as part of the parent unit PA2M/7A.

References to Typical Associated Equipment

1. Central Control Unit UN3/12A

LPB9/72

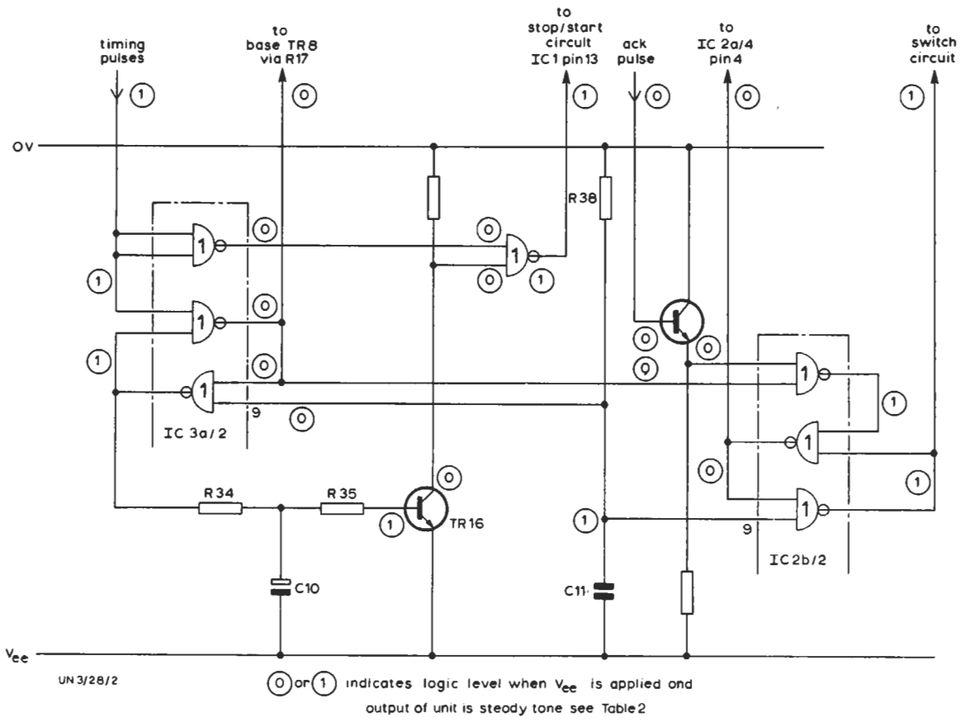

Fig. 3. UN3/28 Tone and Switching Logic Circuit

TABLE 2

Inputs			*Outputs*				
Condition	*Timing pulse*	*Acknowledge pulse to PLA7*	*to stop/start circuit IC1 pin 13*	*to base TR8 via R17*	*to IC2a/4 pin 4*	*to switch circuit*	*Condition*
Unit off							
V_{ee} applied	The voltage across capacitor C11 is initially zero and a logic 0 is applied to pin 9 of IC2b/2 and pin 9 of IC3a/2 to set the correct states for subsequent operations; C11 charges rapidly to a logic 1 level						
	1	0	1	0	0	1	f.m. tone on
1st timing pulse	0	0	1	1	0	1	tone off
	Components C10, R34 and R35 ensure that the logic level at the base of transistor TR16 does not change until after the logic 0 timing pulse has ceased.						
After 1st timing pulse	1	0	1	1	0	1	tone off
No acknowledgement pulse	1	0	1	1	0	1	tone off
2nd timing pulse	0	0	0				V_{ee} off
Acknowledgement pulse received	1	1	1	1	1	0	switch action takes place; pulsed tone on
After acknowledgement pulse	1	0	1	1	1	0	
2nd timing pulse	0	0	0				V_{ee} off