

CONTROL UNIT UN3/525

Introduction

The UN3/525 accepts d.c. and video signal inputs. Certain of the d.c. signals operate relays which are used to switch one of the three video inputs to a single output point. The d.c. switching inputs, together with the other d.c. inputs, are decoded to give a logic signal output in accordance with the decoding. Manually operated switches on the unit allow the automatic switching to be overridden.

The unit is designed for use with a Television Automatic Monitor MN2M/518. It is built on a printed wiring board mounted on a CH1/43B chassis with index pegs in positions 1, 4 and 5.

General Specification

Power Requirements	+12 volts at 80 mA
	+6 volts at 80 mA
	+5 volts at 40 mA

Pin connections 25-way ISEP plug

General Description (Fig. 1)

Video signals are applied to PLA4, PLA6 and PLA8 and the unit switches one of the video signals to an output, on PLA2, in accordance with other received d.c. signals. Table 1 indicates the operating sequence normally employed. Positive logic applies.

Video selection can also be made manually by operating pushbutton switches on the front panel of the unit; each pushbutton incorporates a lamp to show which relay is energised.

Other d.c. signals are applied to PLA12, PLA13 and PLA14. All the d.c. signals are decoded and the correct combinations develop a logic 1 signal at PLA15. See Table 1.

An *Auto* pushbutton switch is fitted and is used in conjunction with other associated units.

Circuit Description (Fig. 1)

Video switching is carried out by means of RLA, RLB and RLC. The relay coils form the collector loads of TR1, TR2 and TR3. A logic 1 signal on the base of one of the transistors energises the associated relay. Contacts on the relays are used to switch indication lamps ILP1, ILP2 and ILP4. The automatic switching can be overridden by manual operation of switches SA, SB or SC.

The logic elements are quad-two input-NAND gates. Gates in circuits IC1b/2 and IC2b/2 are connected as bistable latching circuits.

Test Schedule**Apparatus Required**

- +5 Volt Stabilised Power Supplier
- +6 Volt Stabilised Power Supplier
- +12 Volt Stabilised Power Supplier
- Avometer Model 8

Test Procedure

1. Connect PLA3, PLA17, PLA19 and PLA21 to chassis.
2. Press the *Auto* switch.
3. Check that the *Auto* lamp only is on.
4. Check that all three relays are not energised.
5. Lift pin PLA19 from chassis.
6. Check that relays RLA and RLC are energised.
7. Check that the *Auto* and *Main Feed* lamps are on.
8. Reconnect PLA19 to chassis and lift PLA17 away from chassis.
9. Check relays RLA and RLB are energised.
10. Check that the *Auto* and *Res Feed* lamps are on.
11. Reconnect PLA17 to chassis and lift PLA21 away from chassis.
12. Check that the circuit returns to the state detailed in steps 3 and 4.
13. Operate the *Main Feed* switch.
14. Check that the *Main Feed* lamp is on.
15. Operate the *Res Feed* switch.
16. Check that the *Res Feed* lamp is on.
17. Operate the *Tx* switch.
18. Check that the *Tx* lamp is on.
19. Connect PLA12, PLA13 and PLA14 to chassis.
20. Check that there is a logic 0 signal (0 volts) at PLA15.
21. Operate the *Main Feed* switch.
22. Check that there is a logic 1 signal (+3.0 ±0.5 volts) at PLA15.
23. Connect PLA13 to chassis and lift PLA14 away from chassis.
24. Check that there is a logic 0 signal at pin PLA15.
25. Operate the *Res Feed* switch.
26. Check that there is a logic 1 signal at PLA15.

Reference

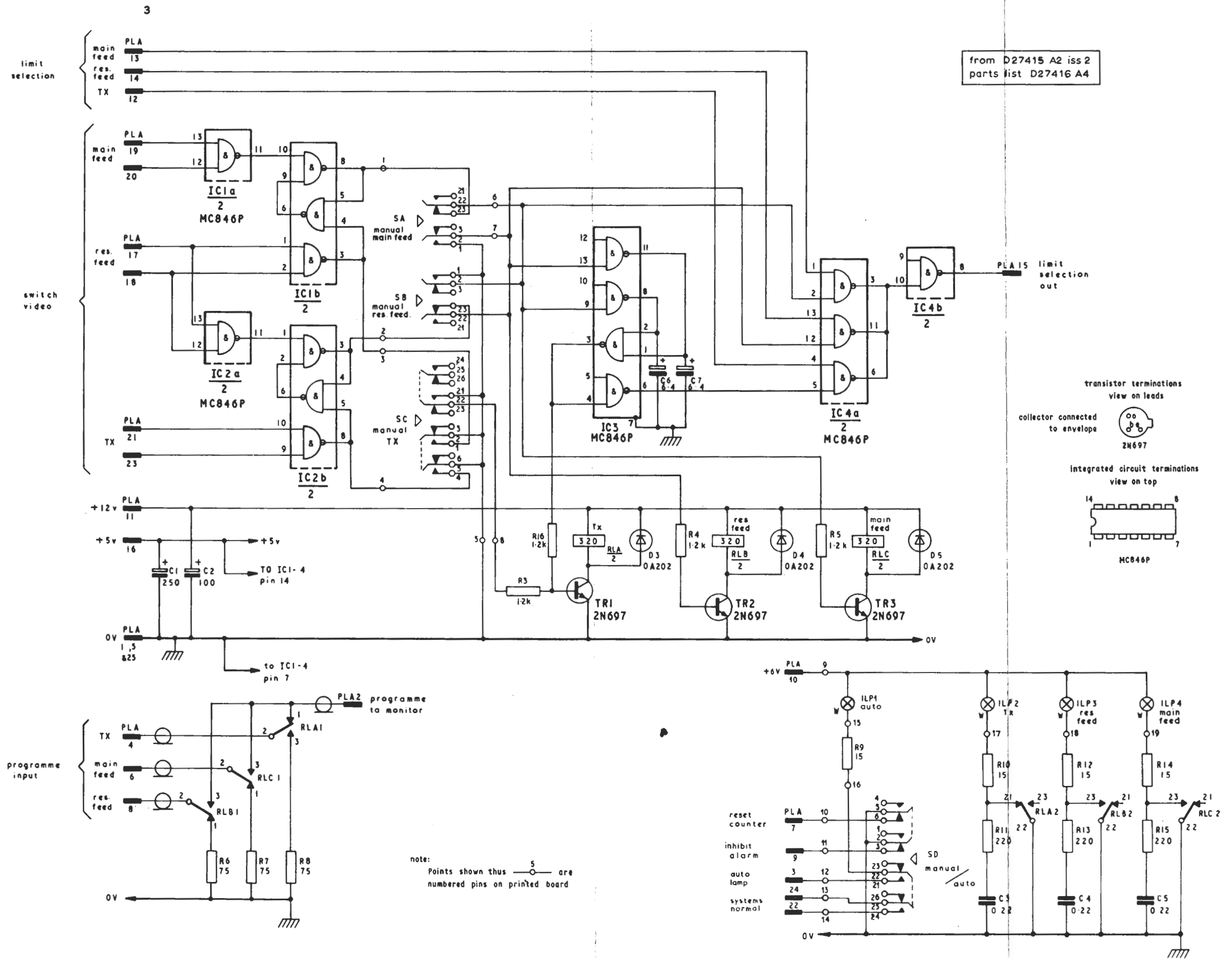
Designs Department Specification 11.103(70).

Reference to Typical Associated Equipment

Automatic Television Monitor MN2M/518.

TABLE 1

<i>Logic 1 inputs to pins:-</i>	<i>Relay energised</i>	<i>Output pin PLA2 fed from pin:-</i>	<i>Indication lamp alight</i>	<i>Logic 1 input at pin:-</i>	<i>Logic 1 output at pin:-</i>
PLA21, 23	none	PLA4	Tx.	PLA12	PLA15
PLA19, 20	RLA, RLC	PLA6	Main Feed	PLA13	PLA15
PLA17, 18	RLA, RLB	PLA8	Res Feed	PLA14	PLA15



from D27415 A2 iss 2
parts list D27416 A4

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Fig. 1.
Circuit of UN3/525