# PAL VECTOR SWITCH UNIT UN9/542

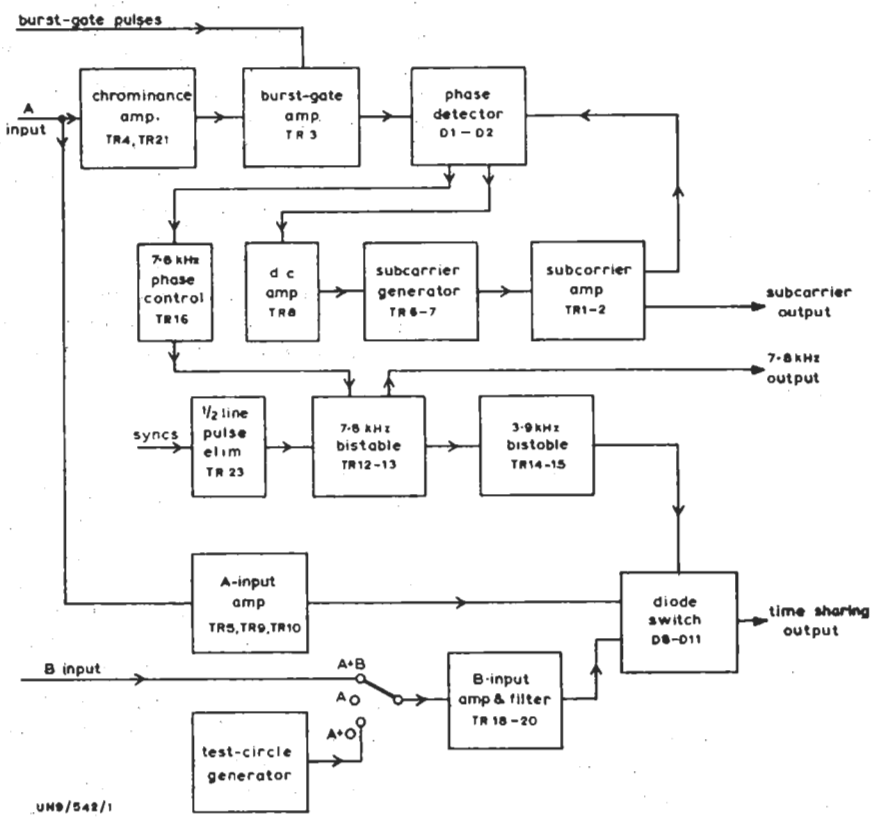


*Fig. 1. Block Diagram of PAL Vector Switch Unit UN9/542*

## Introduction

The UN9/542 accepts one or two composite PAL colour signals, a feed of negative-going mixed-sync pulses[1] and positive-going line-frequency back-porch pulses. It provides: (a) a time-shared output which is switched between two signals at 3·9 kHz[2,3,4]; (b) a 7·8-kHz square-wave signal[2].

From the A-channel colour-input signal the unit regenerates a reference sub-carrier signal. The unit also generates a 4·429-MHz sine-wave signal (used to provide a test-circle facility). This forms part of the time-shared output when the output selection switch is set to *A+0*.

Externally-generated feeds of sub-carrier and 7·8 kHz can be used, if required, instead of the internally-generated signals.

The following controls are mounted on the front panel of the unit:

*Squarewave Int/Squarewave Ext.* (7·8 kHz)
*Sinewave Int/Sinewave Ext.* (sub-carrier)
*Squarewave On/Off*
*A+0/A/A+B* (output selection switch)
*A Gain*
*B Gain*

The unit is mounted on a CH1/12A chassis with index-peg positions 5 and 44.

Power supplies at +6 volts and −6 volts are required[1].

## General Specification

*Input Levels*

| | |
|---|---|
| A and B inputs | 1 volt p-p (composite) |
| Subcarrier | 1 volt p-p |
| 7·8-kHz signal | 1 volt p-p |
| Mixed syncs | 2 volts p-p |
| Burst Gate Pulse | +5 volts |

*Output Levels*

| | |
|---|---|
| Coded output (at 100% saturation) | 1·4 volts p-p (nominal) |
| Subcarrier | 1 volt p-p |
| 7·8-kHz signal | 2·5 volts max. |
| *Subcarrier Frequency* | 4·43361875 MHz |
| *Test Circle frequency* | 4·4296875 MHz (approx.) |
| *A and B Bandwidth* | −3 dB at 800 kHz |
| *A and B Time Input-to-output* | Identical |
| *Power Consumption* | 100 mA |
| *Operating Temperature* | 0–50 °C |
| *Weight* | 1 lb. |

**Circuit Description**

A block diagram which shows the interconnections between the various stages of the unit is given in Fig. 1 and a circuit diagram is given in Fig. 2.

*Chrominance and Burst-gate Amplifiers*

The A-input signal is applied to transistors TR5 (described later) and TR4. The base-bias resistors of TR4, together with the input coupling capacitor form a high-pass network which removes the low-frequency video components from the signal. Transistors TR4 and TR21 form a complementary feedback amplifier and the chrominance signal developed at the output of the amplifier is mixed at the base of TR3 with positive-going back-porch pulses derived from an associated UN1/540 Sync Separator Unit. About 25 volts p-p of colour burst is developed at the collector of TR3 and this is applied, via auto-transformer L2, to the phase detector.

*Phase Detector*

The subcarrier signal present at the collector of TR2 is applied to the detector diodes D1 and D2 together with the colour-burst signal developed across auto-transformer L2. The detector produces two outputs: (a) a d.c. signal proportional to the phase error is developed at the junction of R8 and R9; (b) a burst pulse with alternating phase is developed at the junction of diodes D1 and D2.

*D.C. Amplifier*

The phase-error signal developed at the junction of R8 and R9 is integrated by R34 and C23 and applied to the common-emitter amplifier TR8. The signal appearing at the collector of TR8 is further filtered, to remove any residual 7·8-kHz component, and is then applied to the variable-capacitance diode in the sub-carrier generator stage. The function of diode D13 and capacitor C25, connected between the collector and base of TR8, is to limit the negative rate of change caused by the last burst pulse before the field-sync period; when D13 conducts, C25 limits the gain of the stage by Miller effect[5]. The stage is temperature-compensated by thermistor TH1, which forms part of the collector load of TR8.

*Sub-carrier Generator*

Transistor TR7 is a crystal-controlled common-base oscillator in which the feedback path is controlled by the variable-capacitance diode D3. The capacitance of D3 is determined by the collector potential of TR8 and so provides a very fine control of the frequency of oscillation. The oscillatory signal developed at the emitter of TR7 is applied to the base of emitter-follower TR6. The reference potential applied to the emitter of TR6 by the potential divider R22-R23 is such that the transistor behaves as a common-emitter amplifier at d.c. and applies a feedback signal to the base of TR7; this feedback holds the operating point of the oscillator constant.

The output of TR6 is applied to common-emitter amplifier TR1. Two outputs are taken from the collector load of this transistor; one provides a 1-volt p-p sub-carrier output signal (this replaces the external feed of sub-carrier when switch S3 is in the *Int* position) and the other is fed via common-emitter stage TR2 to the phase detector, described previously, where it is used as the reference sub-carrier signal.

The sub-carrier signal applied to the phase detector completes an automatic phase control loop[6] comprising the sub-carrier generator, the sub-carrier amplifier, the phase detector and the d.c. amplifier.

*7·8 kHz Switch*

A feed of mixed-sync pulses from the associated UN1/540 Sync Separator Unit is applied, via a differentiating circuit and diode gate D14, to a

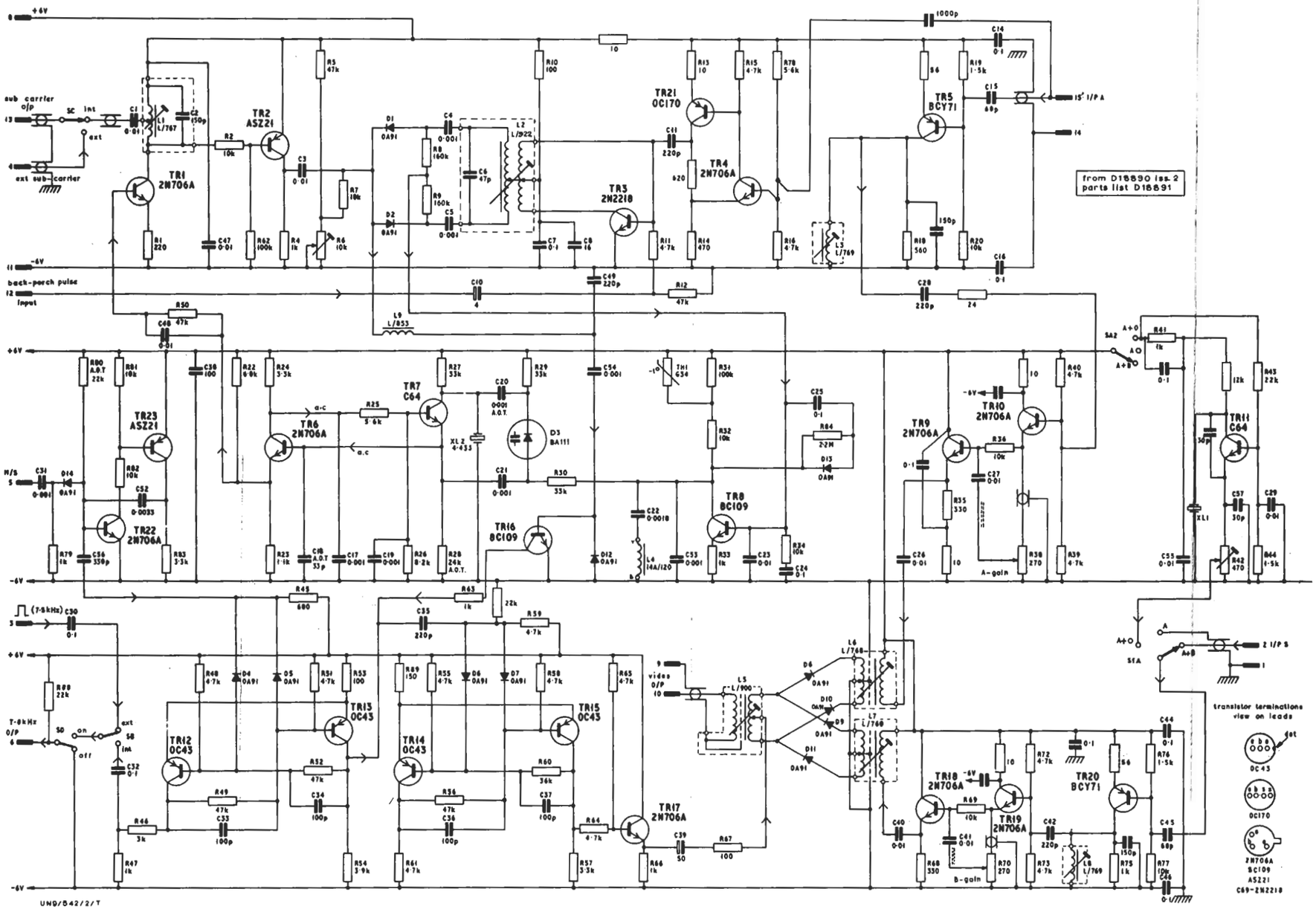




*Fig. 2 Circuit of PAL Vector Switch Unit UN9/542*

monostable multivibrator (see Television Engineering, Vol. 3) comprising complementary transistors TR22 and TR23. The duration of the unstable state is determined by C52 and exceeds a half of one line-period. Thus, during equalising-pulse periods, the multivibrator is in the unstable (cut off) state; this reverse-biases D14 and inhibits the passage of the equalising pulses. When the diode gate is open, differentiated line-sync pulses pass through D14 to the bistable multivibrator TR12–TR13. This multivibrator generates a 7·8-kHz square wave from the leading edges of the applied sync pulses. The phasing of the generator is controlled by common-emitter amplifier TR16. This transistor is fed with the burst-alternating-phase output of the phase detector and clamps the potential at the collector of TR12 in such a way that the bistable stage operates in the correct phase.

The 7·8-kHz output of the unit can be fed either from the internally-generated signal or, if switch S2 is put to the *Ext* position, from an external source of 7·8-kHz pulses. Switch S4 is a mute switch.

*Time-sharing Square-wave Generator*

The 7·8-kHz generator, in addition to providing the 7·8-kHz output, drives a bistable multivibrator comprising transistors TR14-TR15. A 3·9-kHz square-wave signal is developed at the collector of TR15 and this is applied, via emitter-follower TR17, to the centre-tap of output transformer L5. This low-frequency signal switches diodes D8, D10 and D9, D11 alternately into conduction and routes first the A signal and then the B signal to the output transformer.

*Input A and Input B Amplifiers*

The A-input signal is applied to the base of TR5 via a high-pass network formed by the base-bias resistors and the input coupling capacitor; this filter removes the low-frequency components from the input signal and passes only chrominance information. From TR5 the signal is fed via a high-pass filter tuned to sub-carrier frequency to two emitter-follower stages TR10 and TR9 in cascade. The *A-Gain* control is placed at a low impedance point in the emitter circuit of TR10 to minimise changes in phase with changes in gain. The output of the input-A amplifier is applied to the primary winding of transformer L6.

The input-B amplifier, which is similar to the input-A amplifier, develops its output across the primary winding of transformer L7. The amplifier is fed with the B input to the unit only when switch S1 is in the $A+B$ position.

The signals developed across transformers L6 and L7 are coupled to the primary winding of output transformer L5 by diodes D8 to D11 as previously mentioned.

*Test Circle Generator*

Transistor TR11 is a crystal-controlled sine-wave oscillator which produces an output at 4·429 MHz. When this signal is applied to the DM1/502 demodulator a difference-frequency sine wave of about 4 kHz is produced. This provides the contra-rotating test-circle facility for the alignment of the associated vectorscope. The output amplitude is determined by the setting of R42. When switch S1 is in the $A+0$ position the oscillator output is applied, via S1A, to the input-B amplifier. For all other positions of switch S1 the oscillator is muted by the operation of S1B.

**References**

1. Sync Separator UN1/540.
2. PAL Vector Demodulator DM1/502.
3. Vector Detector Unit UN20L/508.
4. Vector Waveform Monitor MN6M/504.
5. Designs Department Technical Memorandum 8.222(66): *PAL System.*
6. Designs Department Technical Memorandum 8.163(64): *Design of Automatic Phase Control in NTSC-type Decoders.*

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