

SUBCARRIER SWITCH UN9/545

Introduction

The UN9/545 accepts inputs of colour subcarrier signal, normal and inverted PAL square-wave signals and burst-gate pulses; it produces colour bursts and four subcarrier signals in the approximate phases of $+(R - Y)$, $-(R - Y)$, $+(B - Y)$ and $-(B - Y)$. It also produces a reference colour-subcarrier signal. Components of the output signals can be switched off by relay circuits for aligning the parent unit.

The UN9/545 is constructed on a CH1/12A chassis with index-peg position 4.

General Description

A block diagram of the UN9/545 is given in Fig. 1. The level of the subcarrier signal fed to the UN9/545 on pin 3 is stabilised in an input amplifier. This amplifier feeds subcarrier signal to a PAL switch and to a 90-degree phase-shift network. PAL square-wave signals also are fed to the PAL switch to invert the subcarrier on alternate lines. The

switched subcarrier signal is fed to a phase-splitting output amplifier to produce phase-alternated subcarrier signals in the $+(R - Y)$ and the $-(R - Y)$ phases.

The output of the 90-degree phase-shift network is fed to a second phase-splitting output amplifier to form subcarrier signals in the $+(B - Y)$ and the $-(B - Y)$ phases, and to a phase trimming amplifier to form an output of reference subcarrier signal.

Feeds of subcarrier signal in the $+(R - Y)$ and the $-(B - Y)$ phases are fed via relay contacts RLD and RLB and via phase-trimming amplifiers to a mixer amplifier. The mixed subcarrier signal is fed to a diode switch together with burst-gate pulses to form the colour bursts.

Circuit Description

The circuit diagram of the UN9/545 is given in Fig. 2 on page 3. The input subcarrier signal is fed via emitter follower TR1 to a class-C amplifier

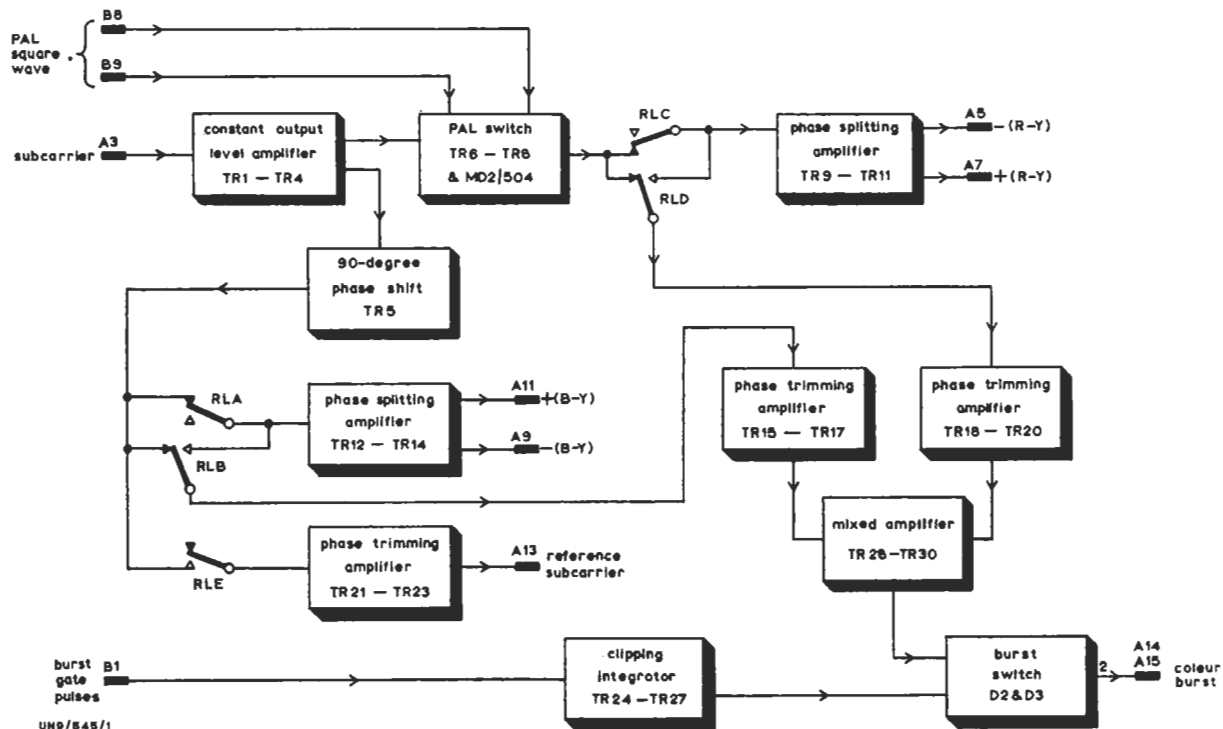


Fig. 1 Block Diagram of the UN9/545

transistor TR2 the output of which is substantially constant. This output is fed to a complementary directly-coupled negative-feedback amplifier, transistors TR3 and TR4.

An output taken from the collector of transistor TR4 is fed to a modulator MD2/504 where it is inverted on alternate lines by the output of a push-pull amplifier (transistors TR6 and TR7) fed with PAL square-wave signals. The phase-alternated output of the MD2/504 is fed via a tuned autotransformer and emitter follower TR8 to the relay circuits feeding a phase-splitting output amplifier. Relay contacts RLC switch off the subcarrier input to this amplifier and relay contacts RLD determine whether the (R - Y) component of the colour bursts is switched off with the subcarrier or remains switched on.

The phase-splitting output amplifier comprises a phase-splitting stage TR9 which feeds two separate emitter followers TR10 and TR11.

An attenuated output of transistor TR4 is fed via a 90-degree phase-shift network* and emitter follower TR5 to a similar arrangement of relay contacts and phase-splitting output amplifier.

The output of emitter follower TR5 is also fed via relay contacts RLE to a phase-trimming amplifier. Relay contacts RLE and RLA are arranged to substitute resistors to maintain a constant load on

emitter follower TR5. The phase-trimming amplifier comprises an emitter follower TR21, a phase-splitting stage TR22 which feeds a series capacitor C34 and C35 and resistor R86.* The junction of the capacitor and resistor feeds an output emitter follower TR23.

Subcarrier signals are also fed via relay contacts RLB and RLD to two other identical phase-trimming amplifiers. The outputs of these amplifiers are added in a shared collector-load resistor of transistors TR28 and TR29. The gains of these transistors are controlled by varying the proportions of their emitter resistors which are decoupled. The mixed subcarrier signal is fed to the burst-gate balanced diode switch via emitter follower TR30.

Input burst-gate pulses are amplified and clipped in transistor TR24 which feeds a pulse-shaping amplifier (transistors TR25 to TR27). This amplifier combines the clipping action of a long-tailed pair amplifier using a constant current source (transistor TR26) and the integration due to the feedback taken from the collector to the base of transistor TR25. The shaped burst-gate pulses are fed to the diode switch.

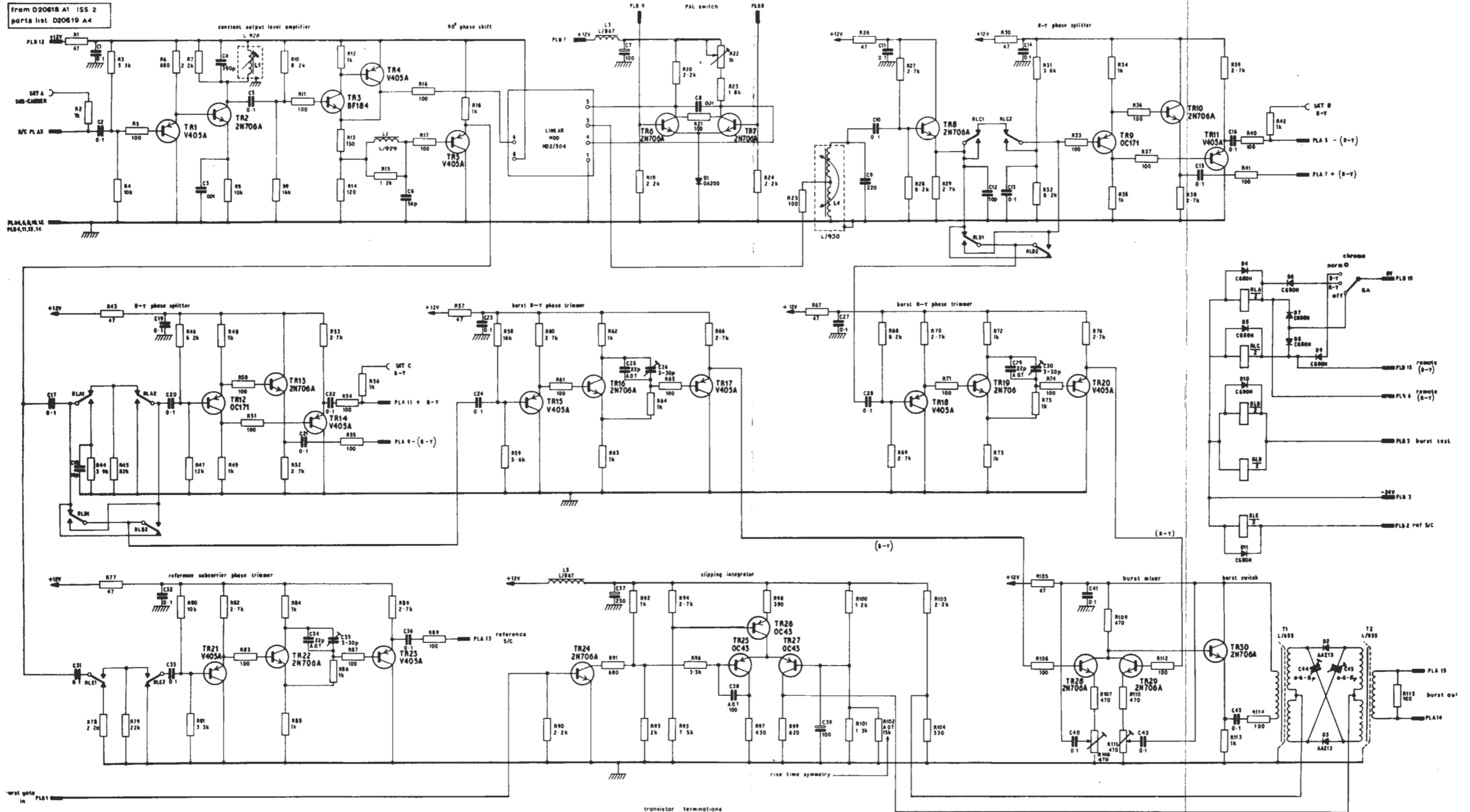
Test Procedure

The UN9/545 is tested as part of its parent unit.

*See Designs Department Technical Memorandum
No. 8.182(65).

MJR 11/67

from D20618 A1 ISS 2
parts list D20619 A4



not gate in PLA1

PLA1 not used

PLA2

UN9/545/ST

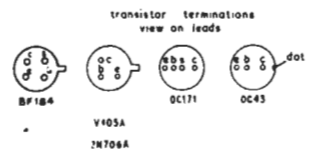


Fig. 2 Circuit of the UN9/545