TECHNICAL INSTRUCTION

GP.5

FERRITE-CORE STORES

SECTION 1

FERRITE-CORE STORES

Introduction

Facilities for the storage and subsequent retrieval of data in the form of binary-coded electrical information form part of certain modern BBC equipments including some computers.

With electro-mechanical systems of information storage such as magnetic tape, the location of the required information takes appreciable time because unwanted information must be scanned before the required section is reached. Where immediate access to stored data is needed, high-speed electronic switching is used and ferrite core-stores are widely employed in such systems. These stores use a number of individual pieces of magnetic material which form the cores of electro-magnets. Each core is capable of registering by the direction of its remanent magnetism either state (0 or 1) of a binary digit (bit). During manufacture a number of these cores are grouped in assemblies a few square inches in area termed matrix-planes. A single matrix-plane can accept or yield only one bit of information at a time; in practical systems groups of bits called words must be handled simultaneously. Thus a complete store system contains several matrix-planes in one or more stacks and cores in the same relative position in each matrix are selected together.

Square-loop Ferrites

The magnetic materials used for the storage are classified as square-loop ferrites because of the shape of the hysteresis loops. The main characteristics of these materials are :

(a) They are magnetically bistable. A magnetising force of saturation strength is required to change the direction of the remanent flux.

(b) Magnetising forces of less than saturation strength have negligible effect on the remnant flux.

(c) The remanent flux is not significantly weaker than that existing when a saturating magnetic force is applied.

Fig. 1 shows a typical hysteresis loop for square-loop ferrite material with points A and B indicating the amount of remanent magnetism. The positive point A could represent the binary figure 1 and the negative point B the binary figure 0. A change from 0 to 1 is made by subjecting the material to a magnetising force of saturation strength and appropriate direction. Current I produces such a magnetising force and with this current applied the flux density reaches point C and drops to point A when the current is removed. Likewise a reverse current of magnitude I would give a flux density of D with a remanent flux of B.

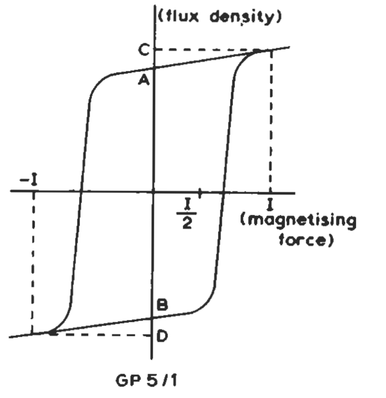

Fig. 1. Typical shape of B–H curve for a square-loop ferrite

Matrix Plane

The cores of elements in a matrix-plane take the form of small rings or beads of ferrite material threaded with wires and are arranged in a grid pattern as illustrated in Fig. 2.

Only 9 cores are shown in the diagram but typical matrix planes in use have 25 to 64 horizontal and vertical rows thus providing storage capacities ranging from 625 to 4096 bits.

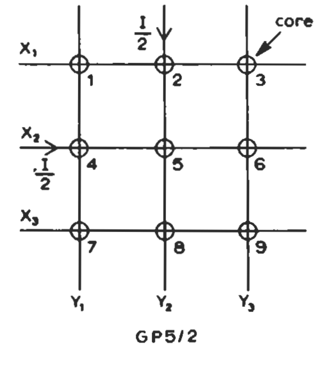

Fig. 2. Arrangement of ferrite cores in a matrix-plane

Operation of X and Y Wires

A current pulse applied to any of the X or Y wires induces a magnetic field in the elements threaded by the wire and if the current pulse is of sufficient strength to cause saturation (I in Fig. 1), all elements in the row will be given a remanent flux in a direction dependent on that of the current. To saturate only one core in the matrix the appropriate

X and Y wires should each be fed with a current of the value required for saturation (known as a half-current and equal to I/2). These two half-currents have the same effect magnetically as a full current through one wire. This is illustrated in Fig. 2 where X_2 and Y_2 have half-currents and core number 5 is thereby switched. The other elements in rows X_2 and Y_2 are subject to a field of only half saturation strength and retain their original direction i.e. are not switched. Pulses applied to individual X and Y wires, appropriately selected, switch any desired element to provide what is called **random** access. Normally information is fed into, or retrieved from, only **one** element in the matrix plane at any time.

Inhibit Wire and Writing-in Process

The switching of elements to the 0– or 1– state by co-incident half-currents in X and Y provides a means of writing information into a matrix-plane. This is done by arranging for directions of the half-current pulses to be positively additive when a 1 is to be written in and negatively additive when a 0 is required.

To enable a number of matrix-planes to be operated on simultaneously (i.e. when a word or group of bits is to be written in) corresponding X and Y wires of each matrix are connected in series and operated from one set of drive-wire circuits. To prevent all matrix-planes being switched to the same logical condition (1 or 0) each has an additional wire which threads all the cores in that matrix-plane.

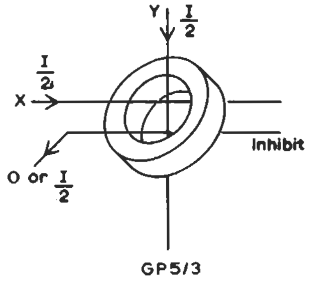

Fig. 3. X, Y and Inhibit wires threading a ferrite core

This is called the **inhibit** wire and its function is to neutralise, if required, the switching effect of half-currents in the X and Y wires. When the information to be stored requires an element to be switched, the inhibit wire carries no current and therefore has no effect on the switching action. If the state of the core is required to be unchanged the switching action is inhibited by feeding a half-current pulse through the inhibit wire so as to oppose the action of the pulse in the X wire. Since the Y wire has a half-current only, the switching action is suppressed.

The above conditions may be summarised by the diagram of Fig. 3. An inhibit wire current of I/2 opposes the X current of I/2 and no switching action occurs.

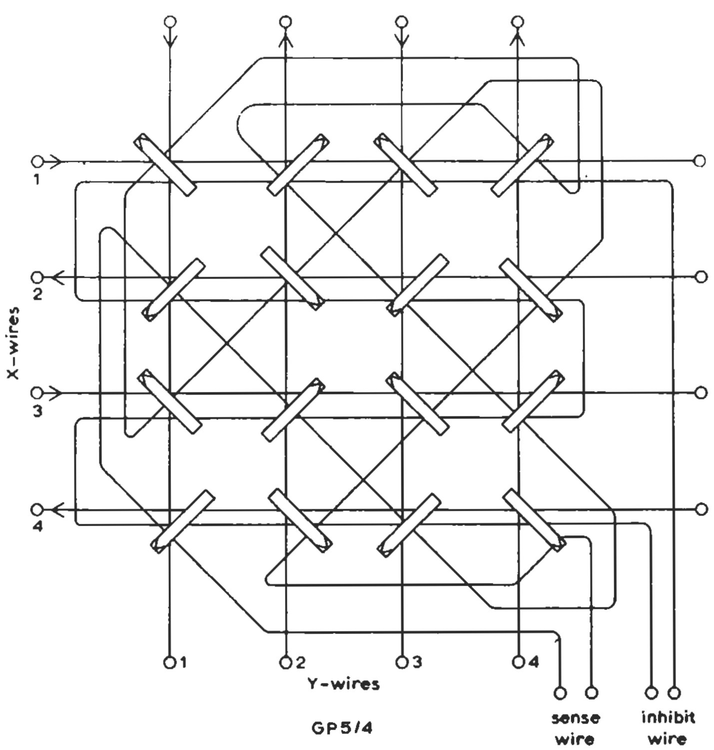

Fig. 4. X, Y, Inhibit and Sense wires threading a simple matrix-plane

Sense-wire and Reading-out Process

To retrieve stored data a further wire is included in the matrix-plane; this is termed the sense wire and, like the inhibit wire, threads all cores in turn, although as shown in Fig. 4 in a different manner to that of the inhibit wire.

Reading-out is achieved by feeding the X and Y wires associated with the core to be read with a half-current pulse of reverse direction to that required for writing in. If the element was switched during writing-in it now undergoes a complete magnetic reversal, producing a pulse in the sense wire, whereas if it was not switched during writing-in, no magnetic reversal occurs and only a small spurious signal is induced in sense wire; this is caused by the small change of flux BD in Fig. 1. The spurious signal would not occur if the section at A and B of the hysteresis loop were truly horizontal.

Although the spurious pulse from a single element is small compared with the pulse resulting from a polarity reversal, the sum of the spurious pulses from all elements subject to half-current pulses could be sufficient to mask the wanted signal. To prevent this the sense wire is threaded so that pick-up from adjacent elements, both vertically and horizontally, is reversed throughout the matrix so minimising the resultant by mutual cancellation. Due to the method of threading the wanted pulses induced in the sense wire may be positive or negative-going. Full-wave rectification is therefore used to produce a uni-directional train of pulses.

Fig. 4 shows a typical arrangement of drive, inhibit and sense wires for a 4 x 4 matrix; a practical matrix would have a much greater number of cores.

Alternate X and Y drive wires require drive currents of opposite direction. This is to enable the inhibit wire to follow a back and forth path through the horizontal rows and maintain the correct polarity. The arrows shown on the rectangles representing the cores indicate relative magnetic polarities, and by following the path of the sense wire it will be seen that the reversal causes cancellation of the spurious pulses throughout the matrix.

The Storage Process

Fig. 5 shows a simple arrangement of three matrix-planes each assumed to contain four cores. The two X and two Y wires are shown threading all three matrix-planes. Each matrix-plane has its individual inhibit and sense wires. Suppose a 3-bit word of the binary form 101 is to be written into the three planes A, B and C respectively. A particular core in each plane is selected by appropriate choice of X and Y drive wires for the half currents. To prevent all three cores (one in each plane) being switched simultaneously a half-current in the correct direction must first be applied to the inhibit wire of plane B to oppose the effects of the X and Y half currents and ensure that this plane remains in the 0 condition. Planes A and B are switched to 1 so that the stored word is 101 as required.

The Read/Write Cycle

As described earlier read-out is achieved by applying half-current pulses to the appropriate X and Y wires. This causes the 'logic–1 information to be erased, a process known as **destructive readout.** In the example given above A and C were in the 1–state and the cores holding this information are switched during read-out to the 0–state. To maintain storage of the information arrangements must be included to re-write logic–1s after readout. This is done by following the read pulses in the X and Y wires immediately by write pulses in the reverse direction and operating the inhibit wire from an amplified and delayed version of the information obtained from the sense wire on read-out. This sequence is called the read/write cycle.

X and Y Wire Grouping

A matrix-plane having a capacity of, for instance, 4096 elements requires internal circuitry capable of switching drive-wire currents to any one of its 64 X– and 64 Y– wires at a time and the most obvious way of doing this is to insert an electronic switch in each of the 128 wires. A more economic and space-saving arrangement is possible by grouping the wires

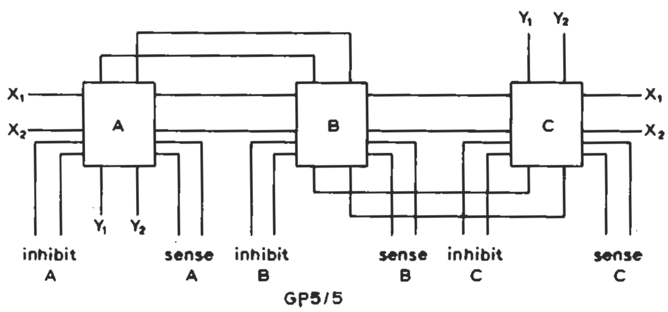

Fig. 5. Arrangement of matrix planes to form a very simple store

and using double switching. This is illustrated in Fig. 6. On the left-hand side of the matrix the wires are formed in 8 groups of 8 wires, with the wires of each group connected together thus providing 8 connection points for the 64 wires. On the right-hand side of the matrix, all number one wires (1, 9, 17, etc.) of each group are connected together, all number two wires, and so on, so as to provide a further 8 connection points. To gain access to a particular wire it is now necessary to select only one of the 8 connections on each side of the matrix, i.e. the system requires 16 switches, compared with 64 required in the original method. A similar set of 16 switches is required for the Y wires. Thus if information is to be written into, or retrieved from the $X_1 Y_1$ Core, switches S1 and S9 for both X and Y wires are closed.

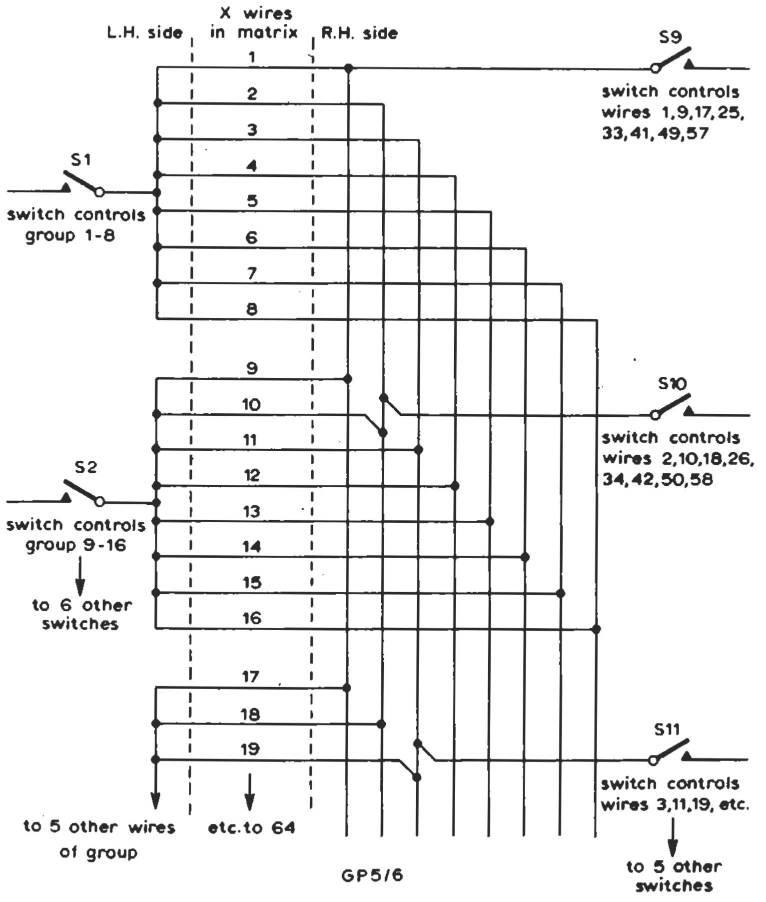

Fig. 6. Method of grouping to simplify X–wire and Y–wire switching

Address Selection

As with any system of storage, precise control of available capacity and accurate retrieval are basic essentials. Therefore associated with every piece of data to be stored must be a reference indicating the location of the information in the store. This is known as the **address location** and is presented to the store in the form of a binary-coded signal which presets a number of high-speed semi-conductor switches and so routes the drive-wire pulses to the appropriate X– and Y– wires. The circuitry performing this function is termed the **address decoding** unit of the store.

Important Characteristics of Ferrite Core Stores

If the ferrite-core method of storing data electronically is compared with other methods, including electro-mechanical processes such as tape recording, the following points emerge:

The ferrite-core store has the following important characteristics:–

- Immediate access to data
- Compact
- Reliable
- Data not lost if supply voltage fails (compare the bistable)
- Expensive.

Generally it is true to say that the ferrite-core store is used where a long-term memory is required (especially where the number of bits is large), but the bistable is used as a short-term memory, i.e. where the time of storage is short.

Acknowledgement

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