DESIGNS DEPARTMENT

DESIGNS DEPARTMENT HANDBOOK

NO.3.130(73)

Handbook on AM6/11 Stereophonic Limiting Amplifier

BRITISH BROADCASTING CORPORATION
ENGINEERING DIVISION

Issue 1
30.1.73

DESIGNS DEPARTMENT HANDBOOK

NO.3.130(73)

Handbook on AM6/11 Stereophonic Limiting Amplifier

.....
(P. DENBY)
for Head of Designs Department

Written by:- M.M. Gleave

RJS

Issue 1
30.1.73

DESIGNS DEPARTMENT HANDBOOK NO. 3.130(73)

Handbook on AM6/11 Stereophonic Limiting Amplifier

C O N T E N T S

D R A W I N G S

30.1.73

DESIGNS DEPARTMENT HANDBOOK NO. 3.130(73)

Handbook on AM6/11 Stereophonic Limiting Amplifier

1. General

The AM6/11 used in conjunction with the UN14/9 delay unit forms a feedforward controlled, overshoot free, stereophonic limiting amplifier designed for use in Broadcasting House Continuity Suites.

For inputs below the limiting threshold of -20dB volume, -12dB peak, both channels have a constant matched gain of nominally +10dB. An output level control is provided by a continuously variable potentiometer enabling the actual below limiting gain to be set in a range of +4dB to -8dB with respect to this.

For inputs up to 20dB above the limiting threshold the output level is held constant to within ± 0.5dB.

The system is arranged such that the gain of both channels in at all times closely matched, and that the degree of gain reduction is determined by the greater of the two stereo inputs.

The system gain and output levels were designed specifically for Continuity Suite use, but below limiting gains up to +20dB and limiting output levels up to 0dB volume could readily be provided with the minimum of modification.

The front panel carries an output level control which for normal Continuity Suite use is set to position N.

A seven position gain recovery switch is also provided enabling the recovery time to be set to 160ms, 330ms, 500ms, 700ms, 1s, 2s and 3s depending on the nature of the programme material being handled.

A front panel meter indicates gain reduction, and provision is made for an external 600Ω 1mA F.S.D. meter to be connected in series with it should remote monitoring of gain reduction be required.

The UN14/9 is housed in a CH1/18C chassis, coding pins 49 and 88 and the AM6/11 in a CH1/37B chassis.

Below is an outline of the systems chief electrical characteristics.

Input impedance	10kΩ (balanced)
Output impedance	40Ω (balanced)
Maximum gain (below limiting)	14dB
Output potentiometer range	12dB
Recovery times	seven fixed values from 160msec to 3 sec. selected on front panel.
Limiting range	20dB
Input threshold	-12dB
Limiting output level (max.)	+2dB
Power requirement	150mA from 24 volt D.C.
Output noise	better than -72dB peaked to '6' with output potentiometer fully up.

Gain reduction may also be brought about by a third audio input providing a 'voice-over' facility. The voice-over input impedance is 10KΩ.

2. Principle of Operation

A block diagram of the system is given in D 33097 A2. Essentially the system may be divided into two parts, the stereo programme chain and the control voltage computation circuitry.

Each programme chain consists of an input transformer, a buffer stage, half the UN14/9 delay unit, a 12dB amplifier, a voltage controlled gain stage, a 12dB range potentiometer and an output amplifier.

The control circuitry takes a signal from the buffer stage at the input of each channel. This signal is in each case amplified and full wave rectified. A threshold reference voltage is generated. Either this reference, or one of the two full wave rectified input signals, is gated through to the input of a fast acting peak detection circuit, depending on which is the greatest at any instant. The output of the peak detector feeds via a buffer amplifier to a pulse shaping network which removes fast changes in the control signal which would otherwise cause unpleasant distortion effects.

Following another buffer stage the signal is fed to the control terminal of the voltage controlled gain stage in each programme chain. Since the programme chain has in it a 330 microsecond delay before the voltage controlled gain stage, any gain reduction can be carried out in anticipation of the input signal thus avoiding overshoot.

The block diagram shows the level at various parts of the circuit when the system is (a) 8dB below limiting threshold (b) at limiting threshold (c) 12dB into limiting.

3. Circuit Description

(a) Rail splitter

Much of the limiters circuitry uses integrated circuit operational amplifiers. These devices require that their differential inputs be biassed midway between the positive and negative rails. Ideally therefore a +12 volt, 0, -12 volt supply is required. The way this is obtained from the incoming 24 volt supply is described below.

R252 and R253, decoupled by C218 and C219, potentially divide the 24 volt rail such that their junction is at +12 volt relative to the negative rail. This forms a reference voltage which biases the non-inverting input of the integrated operational amplifier IC211. The output of this amplifier is connected to the bases of Tr202 and Tr203 whose commoned emitters feed via R251 to the centre rail.

Feedback from the centre rail is applied to the inverting input of IC211. If the centre rail should attempt to become more positive than the reference applied to the non inverting input, the output of IC211 will become negative, switching Tr202 off and causing Tr203 to conduct. Sufficient current will flow via Tr203 and R251 to hold the voltage of the centre rail to within millivolts of the reference voltage. Similarly if the centre rail should attempt to become more negative than the reference, the output of IC211 becomes positive, switching off Tr203 and causing Tr202 to conduct again holding the centre rail close to the reference voltage.

Since the reference is divided by simple potential division of the incoming supply, the centre rail will sit midway between the positive and negative rails over a wide range of supply voltages.

R251 serves to restrict the short circuit current flowing should the centre rail be shorted to either positive or negative rail. A prolonged short circuit may however damage either Tr202 or Tr203.

(b) Programme chain-front end

The main programme chain of each half is identical, this description refers to the left channel but applies equally to the right.

The input is applied to a 2:1 step down transformer T1 which feeds an emitter follower buffer stage. This stage feeds a matching pad which provides a 600Ω source impedance for the following delay line and which also serves to attenuate reflection from the delay line. The return from the delay line is terminated in R113, and feeds the input of a conventional feedback triple amplifier with a gain of approximately 12dB. The precise gain is set by a resistor adjusted on test across R117 soldered between pins 111 and 112 such that with an input of -12.0dB applied to pins PLC13, 14 the output level of this amplifier is -18.0dB ± 0.1dB as measured with a high input impedance amplifier detector across R124 at 1kHz. This adjustment is necessary to make up for the variation in midband through loss of various delay lines. The output of the feedback triple drives the variable gain amplifier via C112.

(c) Variable gain amplifier

IC101, IC102 and IC103 form an amplifier whose gain may be varied between +6dB and +26dB by the application of a d.c. control voltage.

IC101 is a conventional integrated operational amplifier. R127 and R128 provide this amplifier with localised d.c. negative feedback and C114 ensures that localised a.c. feedback is not applied at signal frequencies.

The negative feedback to IC101 is provided via IC102 and IC103. IC102 is a four quadrant multiplier. Over the linear operating region of this device, the differential output appearing across its pins 2 and 14 is linearly proportional to the product of the differential voltages across pins 4 and 8 and pins 9 and 12. Thus:

$$v_2 - v_{14} = K (v_9 - v_{12}) (v_4 - v_8)$$

where K is a circuit constant, here made approximately equal to 0.2 volts $^{-1}$.

v_8 and v_{12} are nominally made equal to zero volts and the audio signal is applied to pin 9. The signal appearing across pins 2 and 14 is now linearly proportional to the d.c. control potential applied to pin 4.

The differential output is applied to the input of the balanced 6dB amplifier formed by IC103. The output of this amplifier drives via R129 into the current summing junction of IC101. The voltage gain between pins 3 and 6 of IC101 is very nearly equal to the reciprocal of the fraction of its output that is applied as negative feedback, and this amount is directly proportional to the d.c. control voltage applied to pin 4 of the four quadrant multiplier. Thus for example if the control voltage is doubled the gain of IC101 is halved.

The actual voltages applied to pins 12 and 8 of the four quadrant multiplier are not exactly zero but are adjusted to compensate for the d.c. input offset voltages of the device. The setting of these voltages is described in Designs Department Manufacturing Information No. 3.558(73) and should not require adjustment after production testing unless IC102 is changed for any reason.

The variable gain amplifier feeds the output level control potentiometer via C122.

(d) Output amplifier

The ganged linear potentiometer R12 allows the level of the two outputs to be controlled over 20dB. R152 and R153 effectively shape the law of the control to be logarithmic. In this way a closer matching of the two stereo halves is achieved than would be obtainable from a conventional logarithmic potentiometer.

The traveller of R12 feeds the non-inverting input of IC104, an operational amplifier whose output drives the base of Tr106. Feedback is taken from the emitter of Tr106 to the inverting input of IC104. IC104 and Tr106 thus form a unity voltage gain amplifier with low output impedance able to drive a 600Ω load via the 1:1 output transformer T4.

(e) Control circuit input

A feed of the input signal is taken from the junction of R108 and R109 and is applied to the non-inverting input of operational amplifier IC201. This amplifier has a gain of 30.5dB bringing the output of this amplifier to -9dB at the onset of limiting (+11dB when 20dB into limiting). This output is a.c. coupled via C221 to a full wave rectifier circuit.

(f) Full wave rectifier

The output of IC201 drives the input of the full wave rectifier. Consider first that part of the circuit comprising R203, R204, R205, D201 and IC202. The voltage on the non-inverting input of operational amplifier IC202 is held at 0 volts by R204. If the output of IC201 goes negative (w.r.t. 0 volts) the inverting input (pin 2) of IC202 tries to go negative. The output of IC202 thus goes positive causing D202 to conduct. Negative feedback is thus applied keeping pin 2 within a few millivolts of pin 3, i.e. 0 volts. Since under these conditions D201 is reverse biassed, the junction of R205, R207 and D201 follows the input voltage in magnitude but with opposing polarity. To this point therefore the circuit acts as an almost ideal half wave inverting rectifier.

The output from this half-wave rectifier is applied via R207 to the inverting input of operational amplifier IC203. The output of IC201 is also applied to this input via R209.

The gain of IC203 for each of these inputs is so arranged that its output equals twice the fullwave rectified a.c. input. Providing at any instant this potential is higher than that provided by the other full wave rectifier or the reference circuit, D204 conducts and applies it to the input of the peak detection circuit via R227. Should either of these other two voltage sources be larger, D204 is reversed biassed, and D203 conducts to maintain negative feedback around IC203.

(g) Reference circuit

In order to obtain a constant below limiting gain and a fixed limiting threshold point a stable d.c. reference voltage is generated. Zener diodes D213 and D214 together with Tr206 and Tr207 form a 'ring of two' stable 5.6 volt d.c. refer nce. This is fed via R225 and R224 to the inverting input of operational amplifier IC207. Providing the output of both rectifiers are below threshold, D211 is cut off, and D210 conducts. Under these conditions IC207 acts as an amplifier with a gain of -0.143. With the stable reference voltage of about -5.6 volts applied to the input, it delivers +0.85 volt to the input of the peak detection circuit. Should at any instant the output of either of the full wave rectifiers exceed this potential D210 is cut off and the appropriate rectifier output is fed to the peak detector.

(h) Peak detection and gain recovery

A positive going peak applied to R227 causes the output of IC208 to swing negative making Tr201 conduct and C212 and C213 to charge via D209. Feedback is taken via the unity gain buffer amplifier IC209 and is applied to the input of IC208. This way C212 and C213 charge to the

peak magnitude, but opposite polarity of the incoming signal. If this peak is short lived the charge appears principally across C212 and thus discharges via R234 with a time constant of 30msec. For inputs driving the device into limiting for more sustained periods the charge distributes itself across C213 also, and now the discharge time constant is formed by C213 and the selected value of gain recovery resistor. A full description of the necessity of such a double time constant is given in Research Department Report No. EL-5.

The output of the buffer amplifier IC209 is fed via the potential divider formed by R236 and R237 to the pulse shaping network formed by L201 and C214. This network reduces the rate of change of the d.c. control voltage, and thus the rate of gain change to a subjectively acceptable value.

The output of the pulse shaping network is fed via the inverting buffer amplifier IC210 to the d.c. control terminal of the four quadrant multipliers in each programme chain, and to the input of the gain reduction meter circuit. This control voltage is approximately equal to +0.36 volts below limiting increasing to ten times this value at 20dBs of gain reduction.

(i) Meter circuit

The d.c. control volts are fed to the input of IC301, an integrated logarithmic amplifier whose balanced output drives the amplifier IC302.

The output of IC302 drives via R308 and R307 to PLC11. Providing links between PLC10 to PLC11 and PLC22 to PLC23 are made the 600Ω resistor R14 completes the circuit through the meter.

If an external 600Ω meter is required links between PLC10 to PLC11 and PLC22 to PLC23 should be omitted and the external meter connected between tags PLC11 and PLC23. R309 sets the meter to 0dB gain reduction below limiting and R308 sets the meter to the 20dB mark at full limiting.

4. Maintenance

The printed circuitry is carried on three boards. Board 1 carries the main stereophonic programme chain and the voice - over input, board 2 carries the gain computation circuitry and board 3 (mounted on the meter) carries the meter drive circuitry.

Below is a brief description on how to firstly determine that a fault condition exists and if so gives some assistance to its identification.

4.1 Below limiting gain

Set the output gain control fully up. Apply an input of -20.0dB at 1kHz to firstly input A and then to input B. In each case the respective output in 600 ohms should be -6.0dB ± 0.2dB. If this is not so first check the voltage appearing on pin 4 of IC102 with respect to pin 215 (for channel A) or on pin 4 of IC106 with respect topin 215 (for channel B). This should be +0.38 volt ± 0.02 V. If this is so then the fault probably exists on board 1 in the relevant programme chain. Levels at various points in this chain should be as follows.

Across the secondary of input transformer	-26.0dB
Across pin 109 and OV rail (Channel A)	-38.0dB ± 1dB
Across pin 139 and OV rail (Channel B)	-38.0dB ± 1dB
Across R124 (Channel A)	-26.0dB ± 1dB
Across R173 (Channel B)	-26.0dB ± 1dB
Across pin 115 and OV (Channel A)	+0dB ± 0.5dB
Across pin 145 and OV (Channel B)	0dB ± 0.5dB
Across pin 119 and OV rail (Channel A)	-6.0dB
Across pin 149 and OV rail (Channel B)	-6.0dB

This procedure should identify the part of the programme chain where the fault has occurred. If the fault is in the region of IC101, IC102 and IC103 on channel A or IC105, IC106 and IC107 on channel B, i.e. on either of the variable gain stages, remove the input and check that pins 6 on IC101, IC103, IC105 and IC107 are at OV ± 100mV w.r.t the 0 volt rail, and that the voltages on the pins of IC102 and IC106 are as shown on the circuit w.r.t the OV rail.

If on the initial test it is found that pin 4 of IC102 or IC106 is not 0.38 volt then the fault probably lies on board 2, or the feed from it, and the following checks are best made:-

Measure the d.c. voltage of the following points w.r.t the OV rail and check that they are as specified

(a)	pin 205	0.38V ± 0.02V
(b)	The junction of L201 and C214	0.38V ± 0.02V
(c)	pin 222	+0.6V ±
(d)	The junction of D213 and R247	-5.6V ± 0.2V

If a fault on either full wave rectifier (IC202 and IC203 for channel A or IC205 and IC206 for channel B) or on the reference amplifier IC207 is suspected switch off the power supply.

Remove links between pins 220 and 221, pins 222 and 223 and between pins 224 and 225. Reconnect the supply and check that with no input the d.c. measured on pin 220 and pin 222 is 0V ± 100mV w.r.t. 0V rail and that pin 225 is at +0.8V ± 1V w.r.t. 0V rail.

The control voltage feed to pin 4 of IC102 and IC106 may be replaced by a feed from pin 158 which should set both channels to approximately their below limiting gain. This provides a means of isolating board 1 from board 2 should this prove helpful.

4.2 Static limiting Characteristic

If the below limiting gain of each channel is satisfactory the static limiting characteristic may be checked by applying an input of -12.0dB at 1KHz and increasing this input in 2dB steps up to +8dB. At each step the relevant output should be +2dB ± 0.5dB. If this is not the case then the fault may well lie in the appropriate full wave rectifier or its drive amplifier (i.e. IC201, IC202, and IC203 for channel A or IC204, IC205 and IC206 for channel B)

With an input of +8dB into either channel, signal appearing between pin 2[illegible] and pin 215 should be as shown in fig 1.

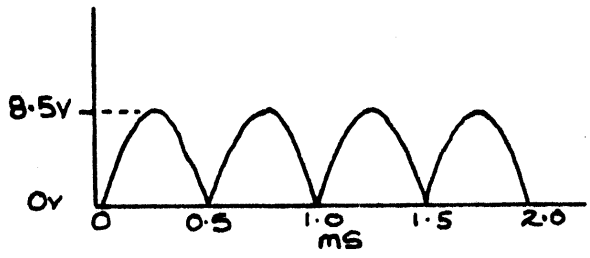


fig. 1

If this is not so, switch off the power supply and remove the links between pins 220 and 221 and between pin 222 and 223. Reconnect supply and with +8dB applied to the input of channel A signal appearing between pin 220 and pin 215 should be as shown in fig 2. Similarly with an input of +8dB applied to the input of channel B the signal appearing between pins 222 and 215 should be as shown in fig. 2

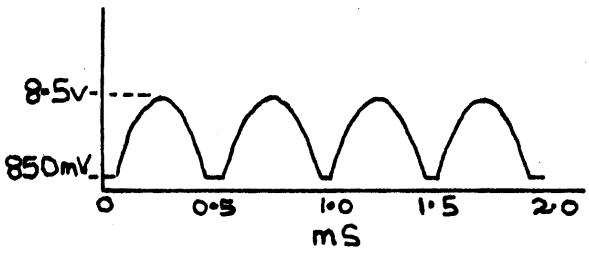


fig. 2

Deviation of the output by more than 0.5dB from the ideal limiting characteristic may also result from the incorrect adjustment of R1114 (channel A) or R1116 (channel B)

These are set up during manufacture and unless IC202 or IC206 is replaced should not require subsequent adjustment. Full details of how they are set up is given in DDMI 3.558 (73).

4.3 Dynamic Limiting Characteristic

The attack and recovery characteristics of the unit are checked during manufacture and few faults can occur in this area of its performance that will not show up as static limiting faults covered in 4.2.

Should for example the gain recovery time appear incorrect or should driving the device into limiting appear to cause a low frequency 'thump' at the output then the unit is best checked by the relevant tests in the production test schedule included in DDMI 3.558(73).

4.4 Voice-over input

To check that the voice-over input is working apply an input of 0dB at 1kHz to the voice-over input and check that the gain reduction meter reads 12dB. With this input the level measured across the secondary of T102 should be -6.0dB.

4.5 Noise

With all inputs terminated in 600 ohm the noise at the output of each channel should be better than -72dB peaked to '6' on a T.P.M and steady to within 2dB.

4.6 Meter circuit

If the performance of the limiter appears satisfactory in other respects the meter circuit may be checked as follows:-
Apply an input of -20.0dB at 1KHz to channel A. The gain reduction meter should read zero. For an input of -12.0dB it should still read zero. Next apply an input of 0dB and +8dB, the meter should read 12dB and 20dB gain reduction respectively.

If either IC301 or IC302 is replaced for any reason the meter circuit may require resetting. This is carried out by adjusting R309 when no input is applied until the meter reads 0dB and then by applying +8dB level at 1KHz to the input of Channel A and adjusting R308 until the meter reads 20dB.

CHANGE
24-4-75

'A' INPUT
Zin=10kΩ
2:1
a) 20dB
b) 12dB
c) 0dB

BUFFER

DELAY LINE MATCHING

330μS
½ UN14/9

a)-38dB
b)-30dB
c)-18dB

12dB

VARIABLE GAIN STAGE

a)-26dB
b)-18dB
c)-6dB

6dB

a)-32dB
b)-24dB
c)-12dB

FOUR QUAD
MULTIPLIER

a)-10dB
b)-2dB
c)-2dB

1:1
'A' OUTPUT
Zo=40Ω
a)-10dB
b)-2dB
c)-2dB

VOICE OVER INPUT
Zin=10kΩ
2:1

BUFFER

a)-17dB
b)-9dB
c)+3dB

FULL WAVE RECTIFIER

CONTROL VOLTAGE GATE

+860mV

THRESHOLD REFERENCE

PEAK DETECTION AND GAIN RECOVERY NETWORK

BUFFER

PULSE SHAPING NETWORK

BUFFER

a)+380mV
b)+380mV
c)+1.5V

LOG. AMP.

METER DRIVE

a) 0mA
b) 0mA
c) 540μA

GAIN REDUCTION METER

24VOLT
+
-

RAIL SPLITTER

+12V
0V
-12V

a) SYSTEM 8dB BELOW LIMITING THRESHOLD
b) SYSTEM AT LIMITING THRESHOLD
c) SYSTEM 12dB INTO LIMITING
N.B. IN ALL CASES OUTPUT POT. ASSUMED SET TO 'N'
D.C. VOLTAGES ARE W.R.T. 0 VOLT.

'B' INPUT
2:1

BUFFER

DELAY LINE MATCHING

330μS
½ UN14/9

12dB

6dB

FOUR QUAD
MULTIPLIER

1:1
'B' OUTPUT

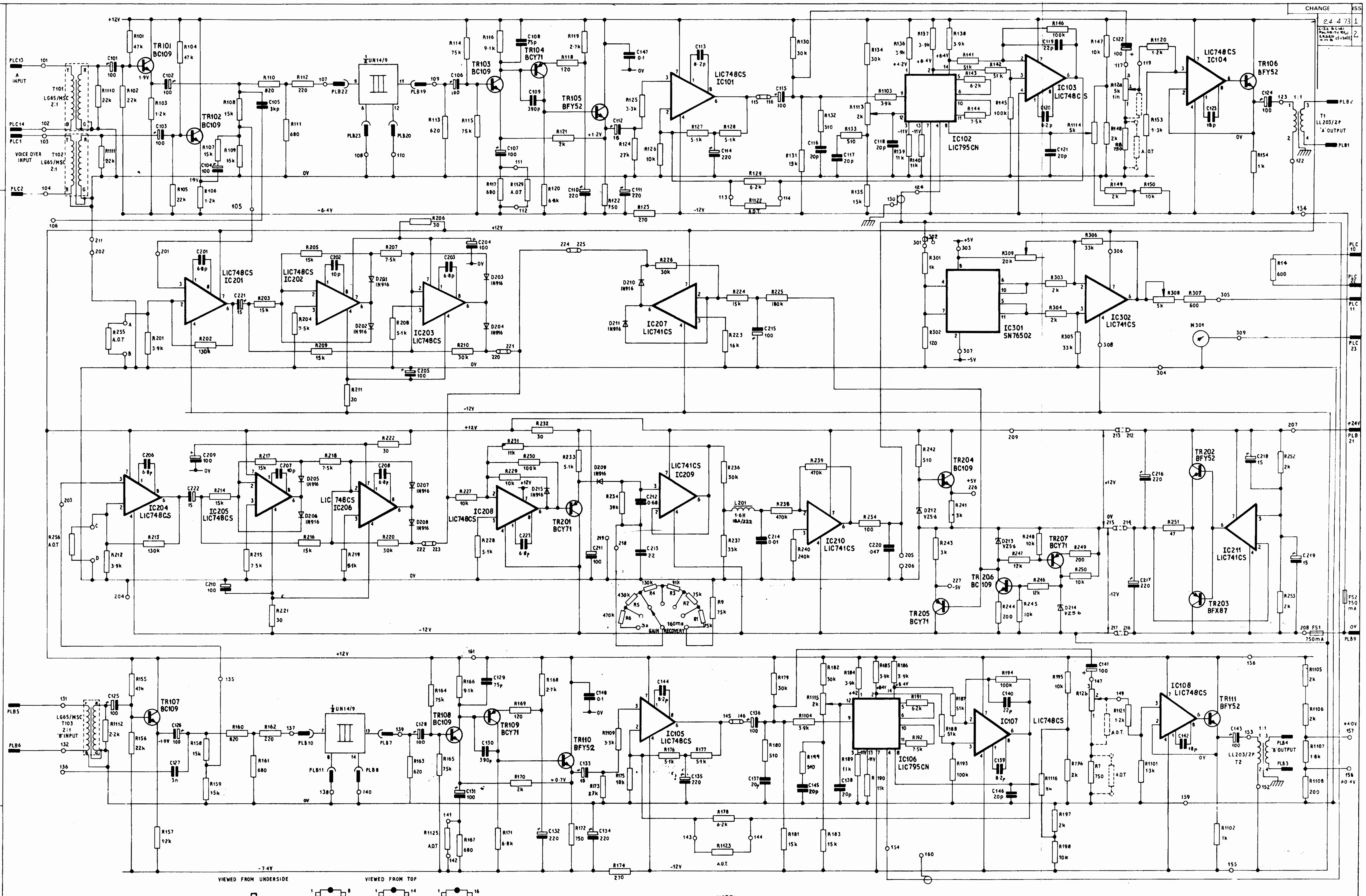
3.130

D33097 A2 AM6/11 STEREOPHONIC LIMITING AMPLIFIER BLOCK DIAGRAM

BBC DS/A2

AM6/11 STEREOPHONIC LIMITING AMPLIFIER BLOCK DIAGRAM

DRN.	D.E.G.	designs department
TCD.	P.J.	D33097 A2
CKD.	M.W.G.	
APPD		



NOTE:-
COMPONENT NUMBERS IN SERIES 0-20 i.e. R1 WILL BE LOCATED ON REAR OF PANEL
" " " " 100-199 & 1110-1126 i.e. R101 & R1101 WILL BE LOCATED ON BOARD No. 1
" " " " 200-256 i.e. R201 WILL BE LOCATED ON BOARD No. 2
" " " " 300-301 i.e. R301 " " " " " No. 3

PARTS LIST :- D33079A4

BBC

DS/A1

AM6/11 STEREOPHONIC LIMITING AMPLIFIER CIRCUIT

DRN.	DEG	DESIGNS DEPT
TCD.	PJ	
CKD.		D33078A1
APPD.		